Exhibit 2 Function of Each Active Circuit / Circuit Diagrams : 2.983 (d)-9, 7, 11

Exhibit 2 provides technical information on the function and design of each of the active circuits used in the Active Antenna. Specific items included in Exhibit 2 are listed following

Included Items

1. HPA Circuit Card Assembly (CCA)
2. LNA Circuit Card Assembly (CCA)
3. DC / Fault Circuit Card Assembly (CCA)
4. Calibration Circuit Card Assembly (CCA)
5. Bandpass filter characteristics (2.983 (d) -11)

2-1 HPA Circuit Card Assembly (Power Amplifier, 2.4 Watt, Qty 3 per Channel)

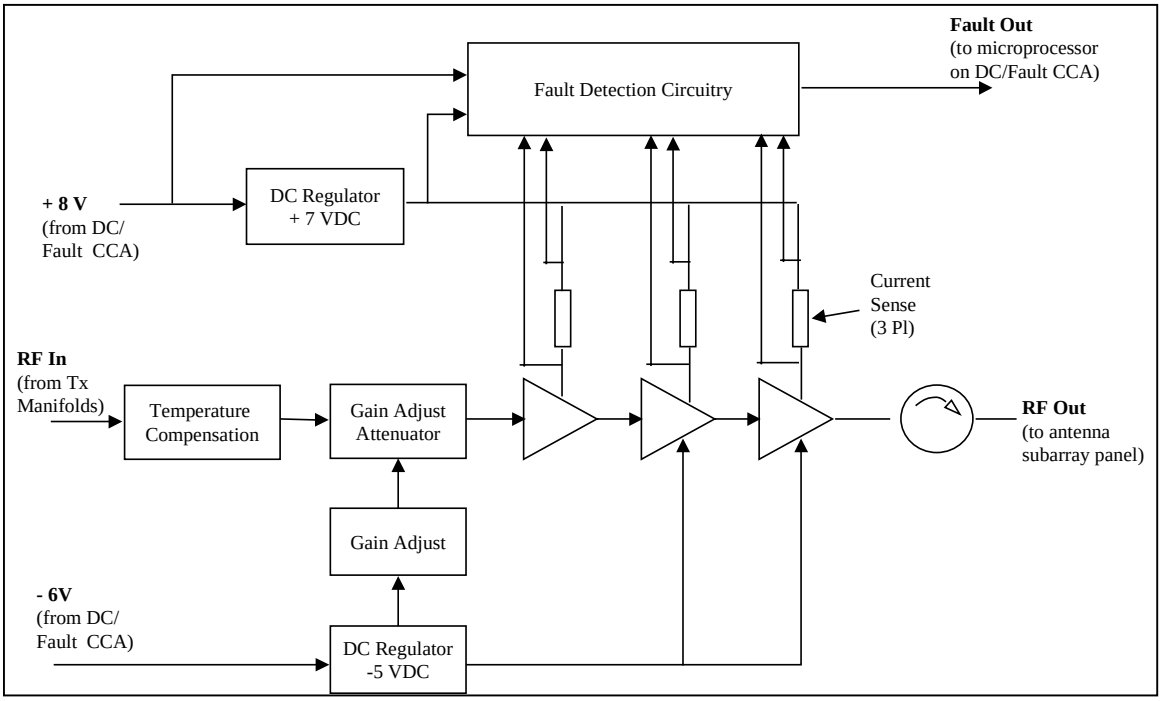

Figure 2-1 HPA CCA Block Diagram

Three high power amplifier (HPA) cards are used in each transmit channel. Figure 2-1 shows a block diagram of the HPA circuit card assembly (CCA). Each HPA CCA is a three stage linear power amplifier with a rated power output of 35.5 ± 0.5 dBm. All three stages are Gallium Arsinide (GaAs) HFET type devices. The CCA includes on board power regulation, current sensing for fault isolation, an output isolator, and an adjustable attenuator used during manufacturing to adjust the power output to the nominal value noted. The input to the amplifier is through a 7db temperature compensating attenuator with a .007 dB/dB °C slope to flatten the response. The compensated amplifier produces the maximum output power at room temperature, where the output power is adjusted, and falls off at either temperature extreme. (See Figure 4-2 in Exhibit 4 for the amplifier's temperature response.) The CCA uses 100% surface mount components. Circuit schematics are provided in Exhibit 3 and a photograph is included in Exhibit 9.

2-2 LNA Circuit Card Assembly (Low Noise Preamplifier, Qty 3 per Channel)

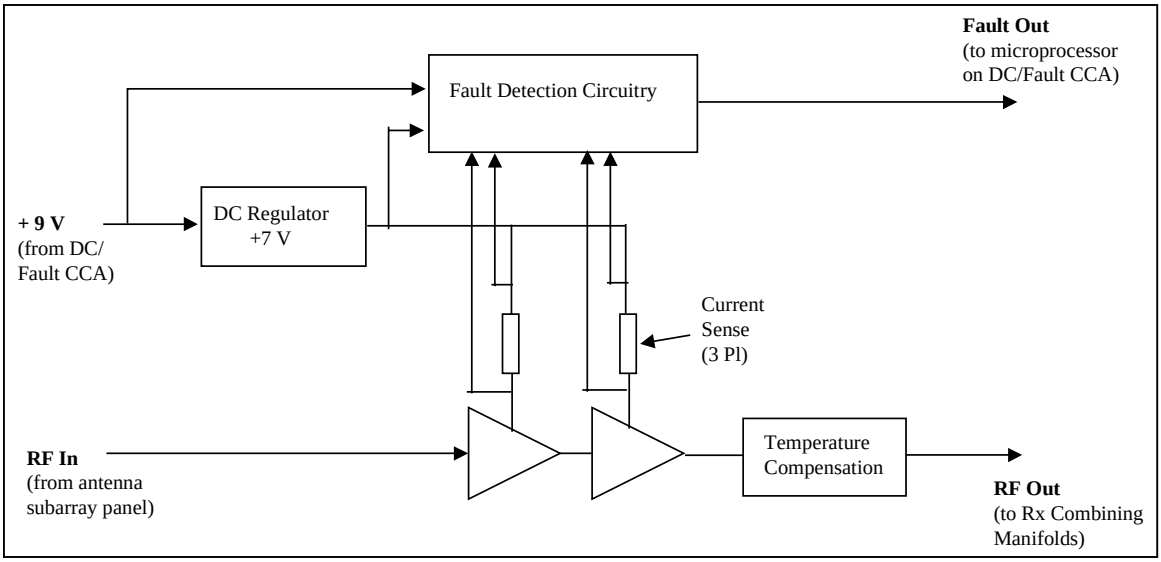

Figure 2-2 LNA CCA Block Diagram

Each of the two receive diversity channels utilizes three low noise amplifier (LNA) cards. Figure 2-2 shows a block diagram of the LNA circuit card assembly (CCA). The LNA CCA is a two stage low noise amplifier with a rated gain of approximately 26 dB. The CCA includes on board power regulation and current sensing for fault isolation. The CCA uses 100% surface mount components. Photographs and circuit schematics are shown in the "Internal Components" and "Schematics" exhibit files.

2-3 DC / Fault Circuit Card Assembly (Qty 1)

The Active Antenna is powered by a DC/Fault circuit card. This card accepts the –48VDC prime power input supplied by the PBC and provides regulated, filtered drive voltages for the HPA and LNA circuit cards. Two redundant power supplies and filtering circuits are packaged on a single card to improve overall reliability of the system. If the primary supply fails, it is switched offline and the redundant supply takes over.

Figure 2-3 shows a block diagram of the DC suppy portion of the circuit card. It contains switching DC - DC power converters running at 250 / 500 KHz, power regulation and filtering circuits, and surge suppression circuits.

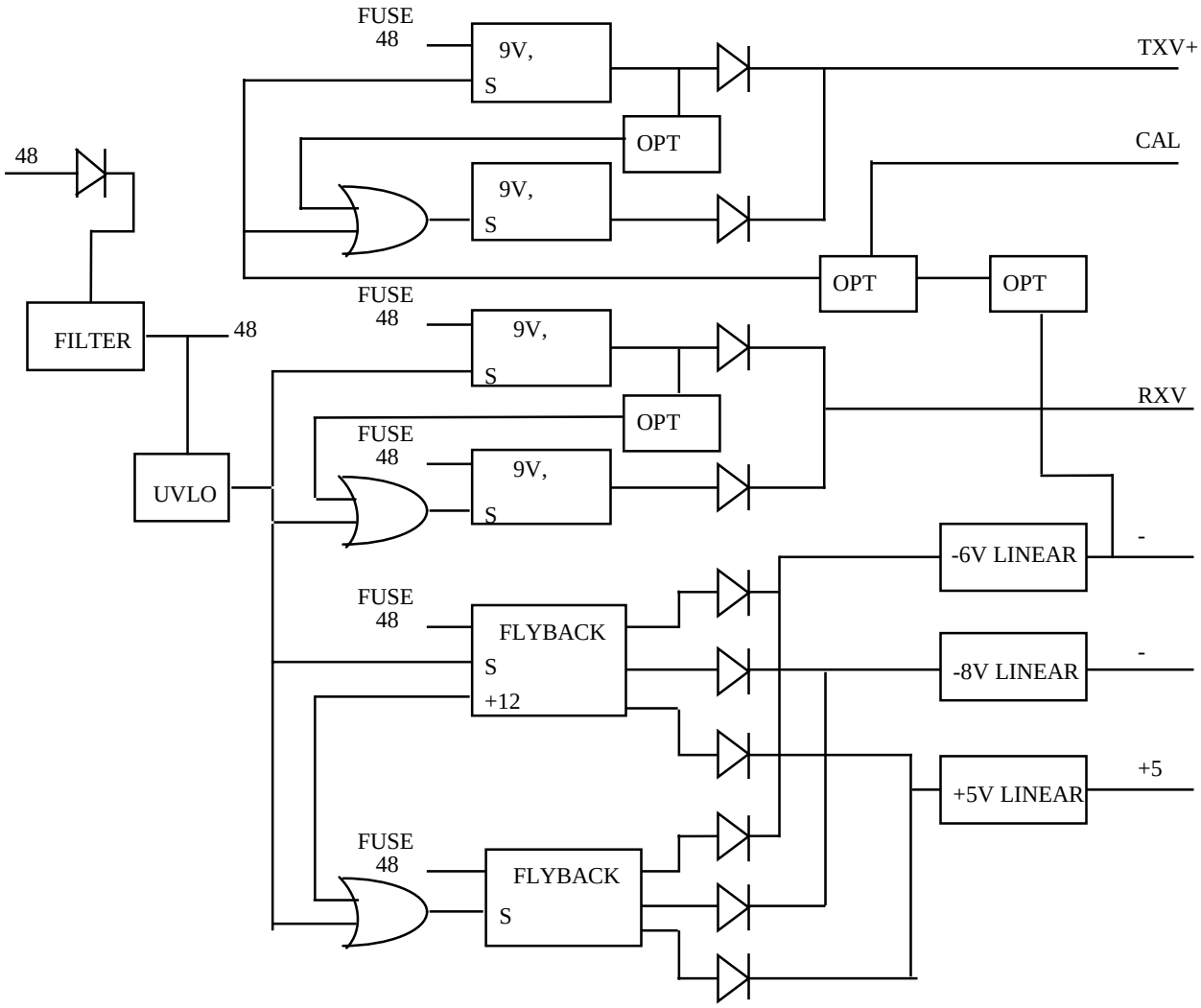

Figure 2-3 - DC/ Fault CCA Block Diagram

The DC/Fault card also hosts the system control microprocessor. The microprocessor is a 16 bit Motorola 68HC12 running at 16 MHz. It handles the control commands from, and responses to the PBC via an RS-485 data link which runs over a single shielded twisted wire pair.

During normal operation, the processor monitors discrete fault lines from the power supply and each of the amplifier circuits. It formats this information into two, 16 bit alarm response words that are supplied to the PBC upon interrogation, approximately once per second.

On operator command, via the PBC control panel, the processor will also: supply the software version number, disable the HPA's (in preparation for calibration), set the internal attenuators to the proper drive level, re-enable the HPA's, set the internal attenuators to maximum (normal position when leaving the factory), and download an event log containing a limited history of commands, responses, and alarms.

When commanded to set the attenuators, the controller begins the calibration sequence by automatically resetting the attenuators to their maximum value. It then steps the value down until a logic signal from the detector in the calibration circuit (see section 2-4) indicates that the drive level is correct to generate a 500 W EIRP signal from the HPA's. The required attenuator setting for each channel is then written to non-voltile memory. If an acceptable level is not found, the attenuators are returned to the maximum value and a fault message is sent to the PBC.

Circuit schematics are included in Exhibit 3 and a photograph of the card is shown in Exhibit 9.

2-4 Calibration Assembly (Qty 2, 1 per channel)

Figure 2-4 shows a block diagram of the Calibration CCA. The calibration circuit for the Maxite system adjusts the input drive level so that the radiated power out of the amplifiers is 38.5 dBm ±0.3 dB at 25 C with any feeder cable loss between 0 and 12 dB between the Active Antenna Unit (AAU) and the radio Base Station (RBS). The calibration circuit has a temperature compensated detector that is factory set to trip a logic flag at nominal power level. It also has an attenuator that compensates for the feeder loss according to the following equation:

Feeder loss (in dB) + attenuation (in dB) = 12.

The attenuator has 0.5 dB steps and is initially set to maximum attenuation. During calibration, the RBS is set to it's standard operating power of 32.5 dBm out at the center of the applicable transmit band. The system is then calibrated under software control by reducing the attenuation in 0.5 dB steps until the detector trips. The attenuator setting is stored in non-volatile memory, to be recalled in case of power failure

Circuit schematics are included in Exhibit 3 and a photograph of the card is shown in Exhibit 9.

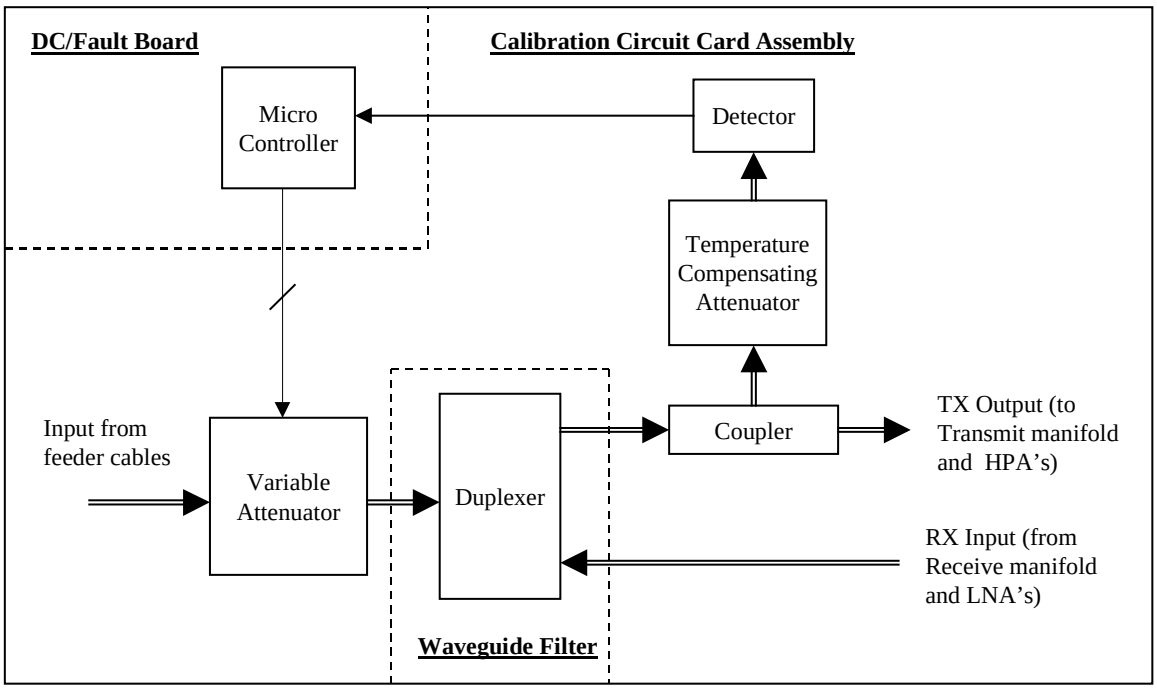

Figure 2-4 Tx Limit CCA Block Diagram

2-5 Bandpass Filter Characteristics

Figures 2-5 through 2-7 show the RF response of each of the three passive filters that correspond to the three dash numbers of the Active Antenna covered by this application Figure 2-8 shows the wideband response of a typical transmit filter. As can be seen in the figures, the filters demonstrate the same characteristics in each of the three passbands shown, with one exception. An additonal pole has been introduced in the Band 1 transmit and Band 3 receive filters to provide a sharper response at the band edge. This provides more margin for "A" band intermodulation products that may be present present in the adjacent "F" receive band, if two high power antenna systems (one from each block) were to be co-located.

The transmit filters have been designed to limit out-of-band emissions by a minimum of 30 dB to ensure compliance with the –51.5 dBc (-13 dBm) limits specified in 47 CFR 24.238 and the -36 dBm limits specified in paragraph 5.3.5.2 of the JTC standard for GSM equipment providers, J-STD-007A - PCS Air Interface Specification. In addition, these filters attenuate reverse intermodulation products in the receive band so that, in conjunction with the HPA's double junction circulator, the reverse intermodulation products generated are less than –100 dBm/100 kHz under the test conditions specified in J-STD-007A, paragraph 5.3.9.2. This ensures that the RBS/AAU system will comply with the –98 dBm reverse IM level specified for GSM equipment providers.

Receive filters have been designed to attenuate transmit energy by an additional 30 dB. This, in conjunction with the isolation between the two antenna apertures, ensures that the residual transmit signal at the output of the receiver preamplifiers will not compress the receiver in the radio base station.

Circuit schematics are included in Exhibit 3 and a photograph of the card is shown in Exhibit 9.

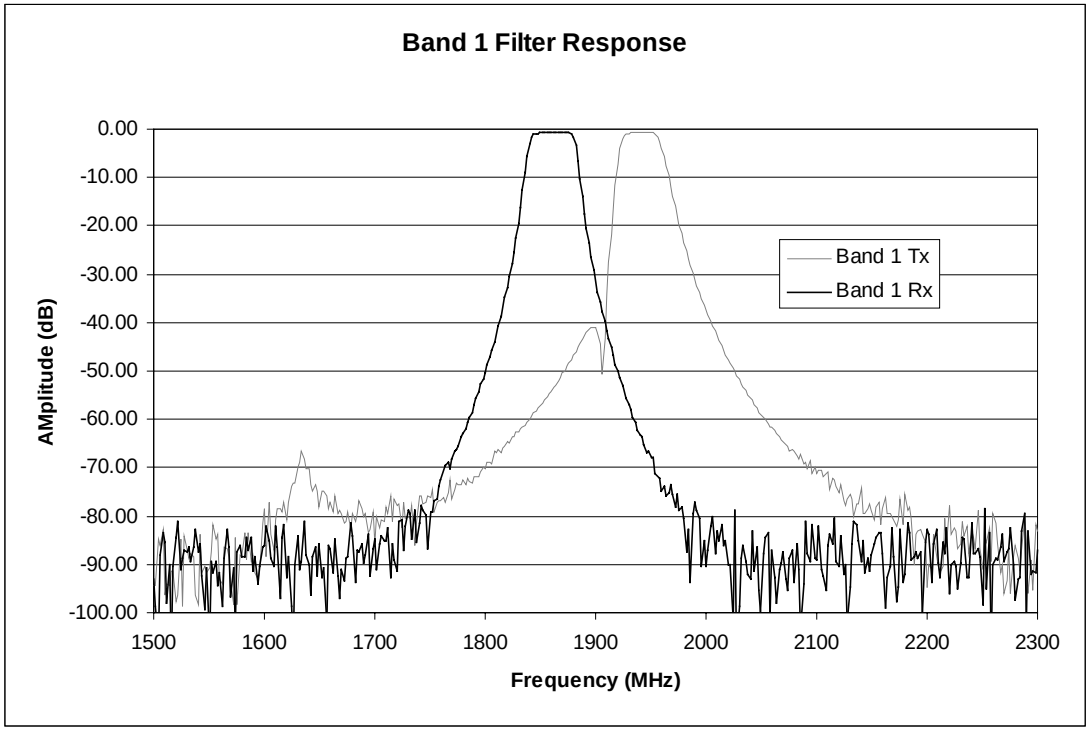

Figure 2-5 Band 1 Filter Response

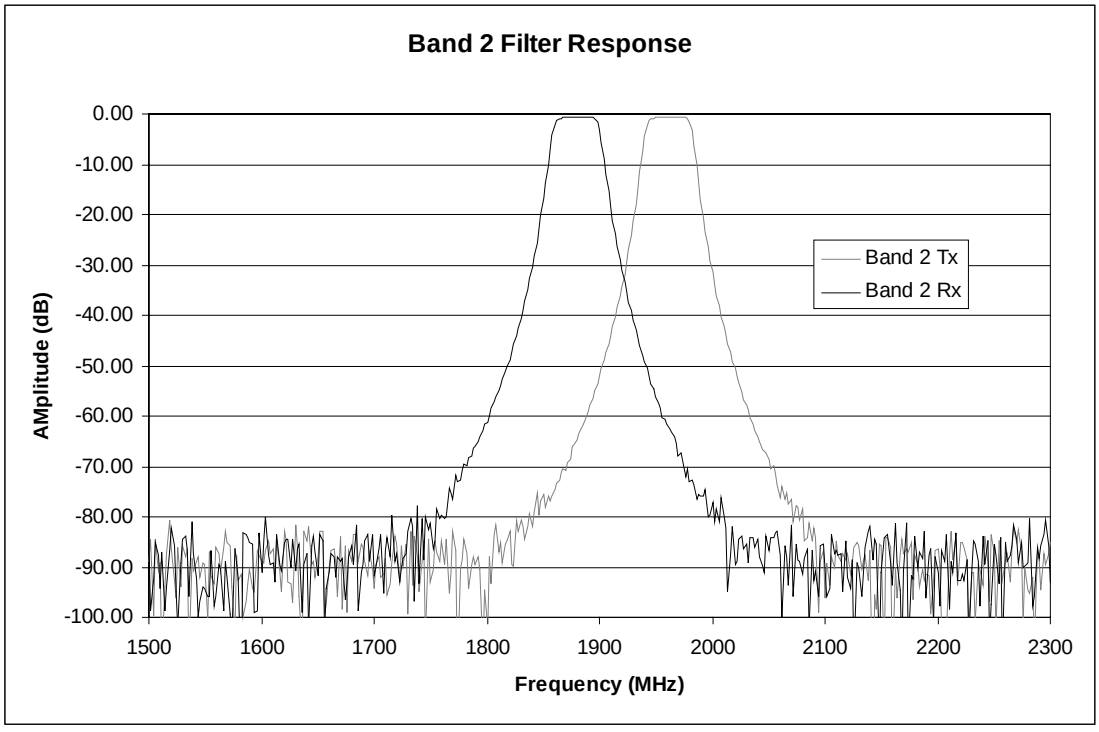

Figure 2-6 Band 2 Filter Response

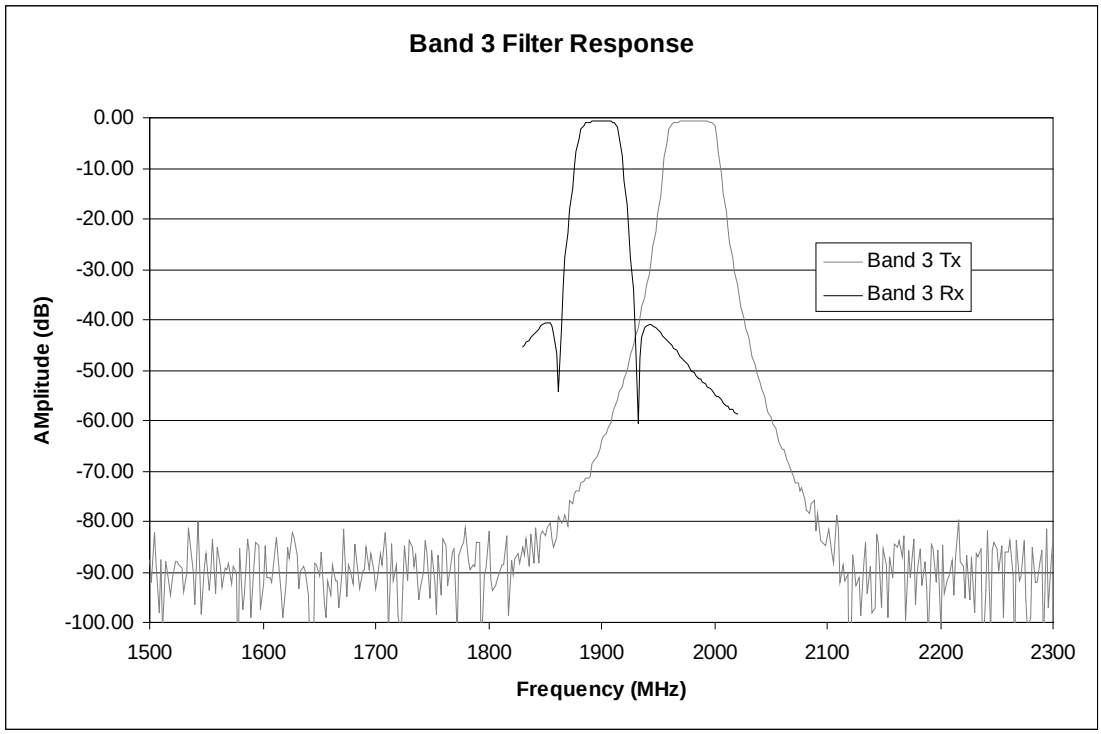

Figure 2-7 Band 3 Filter Response

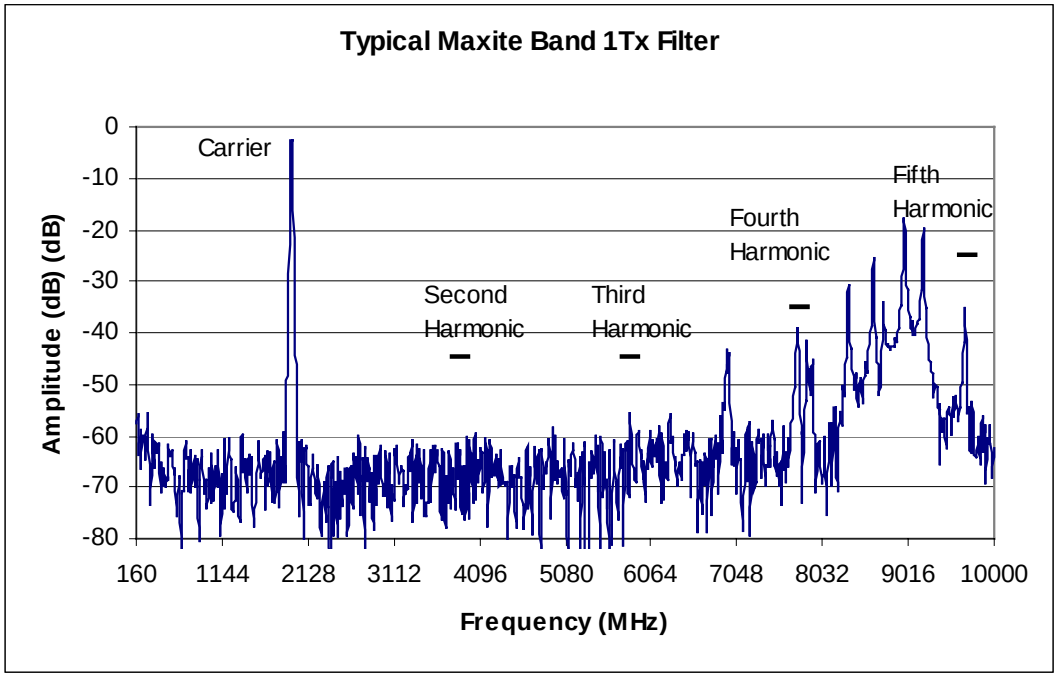

Figure 2-8 Wideband Response ofTransmit Filters (Band 1, Typical)