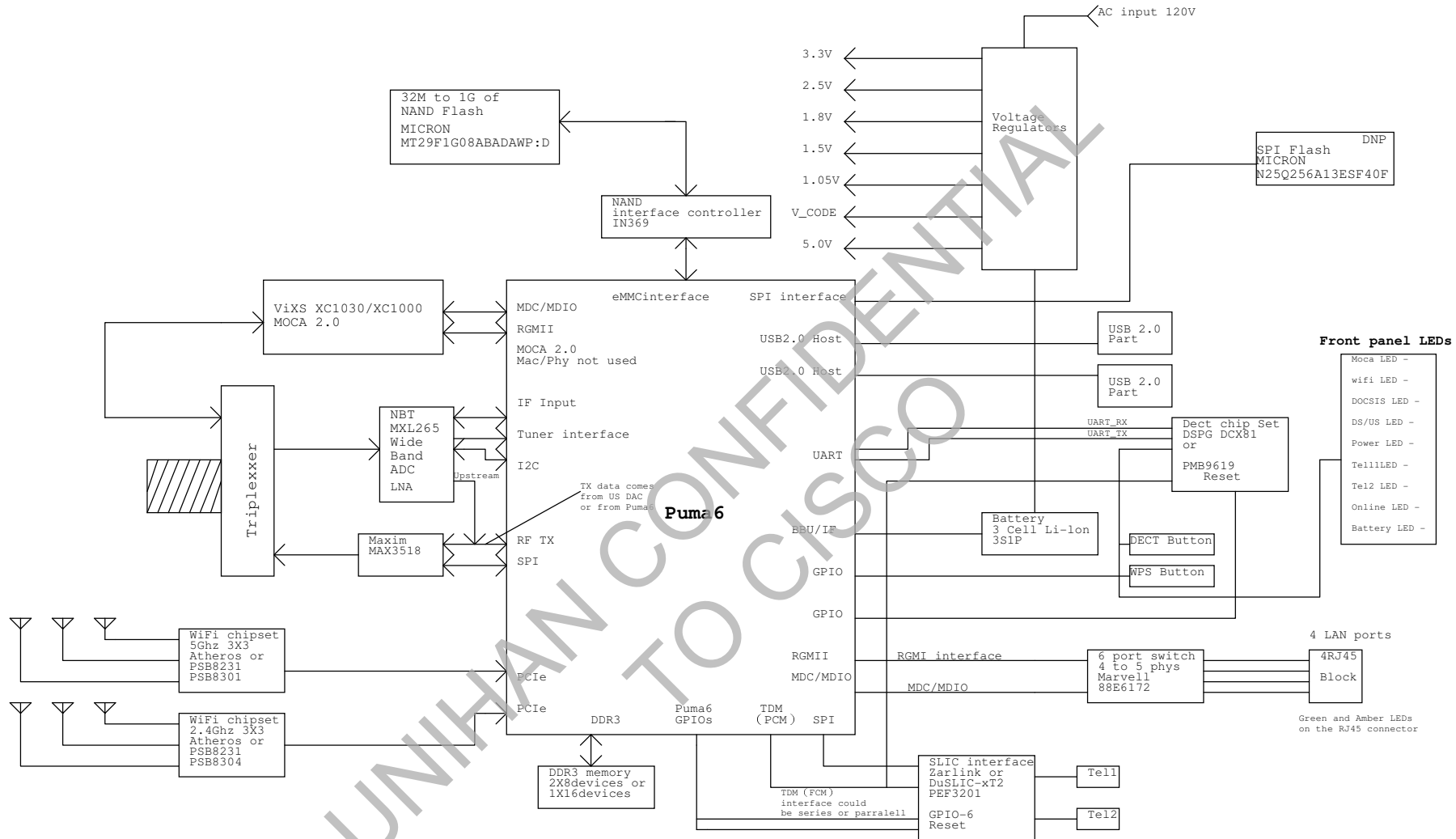
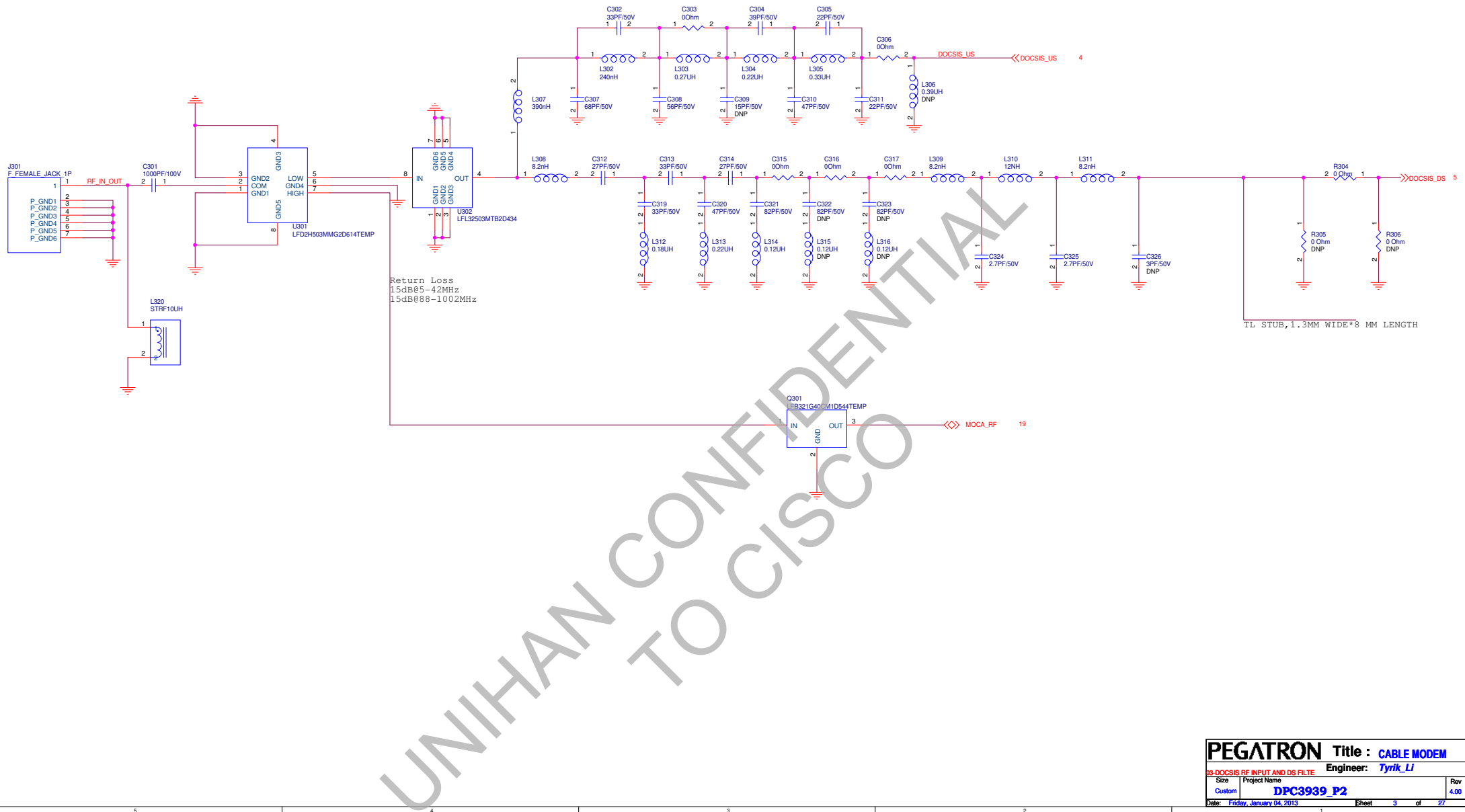


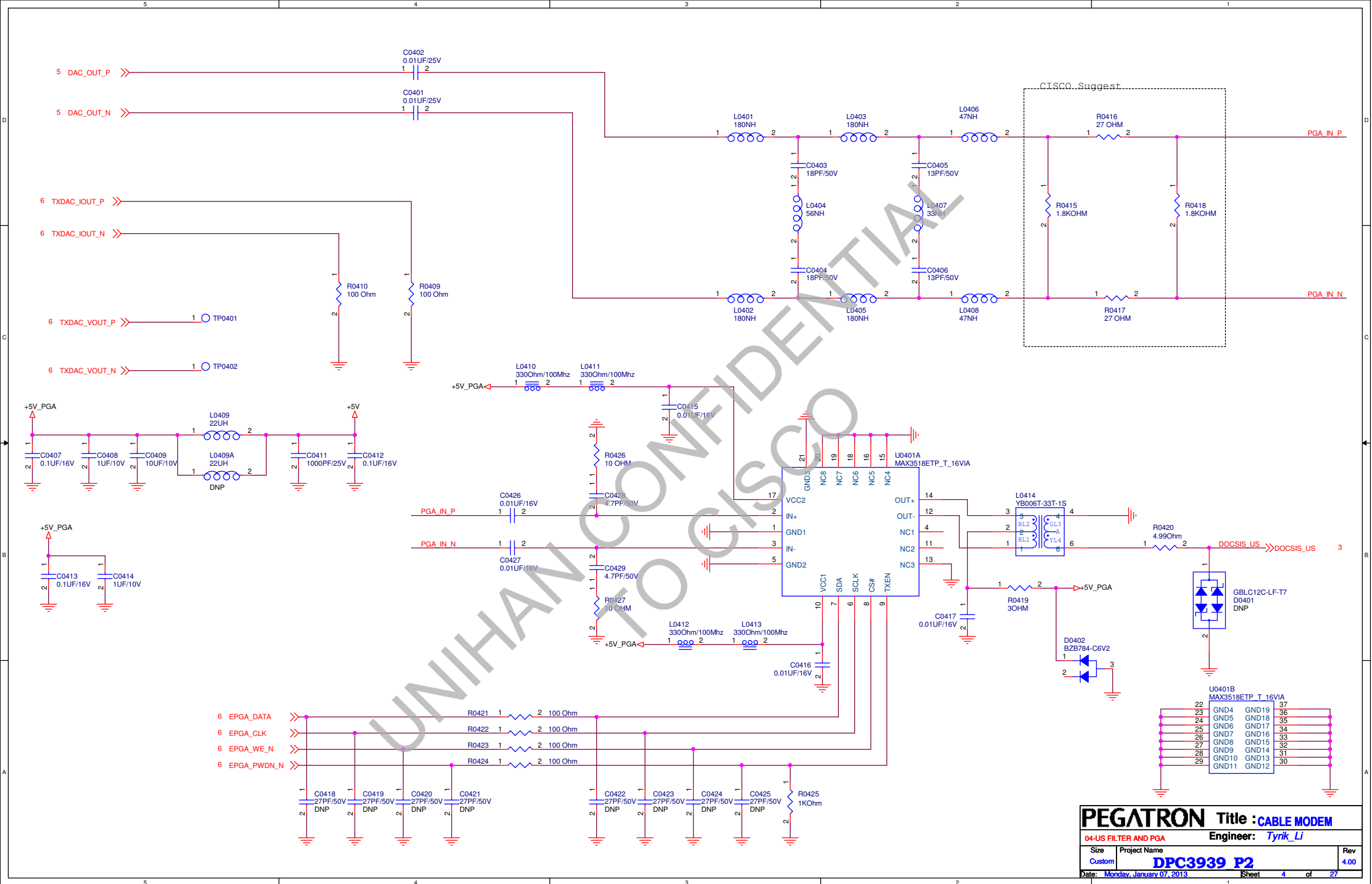
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4	US FILTER AND PGA
5	WB/NB TUNER AND POWER
6	ADC
7	POWER AND POWER FILTER
8	GND
9	DDR3 INTERFACE AND MEMORY
10	GPIO,LED BUTTONS SWITCH
11	USB PORT
12	ETHERNET SWITCH
13	SPI FLASH AND NAND FLASH

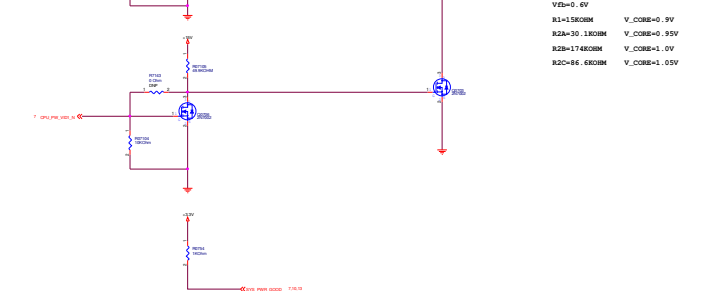
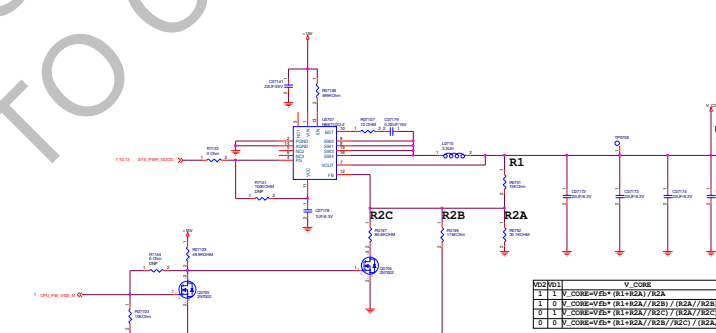
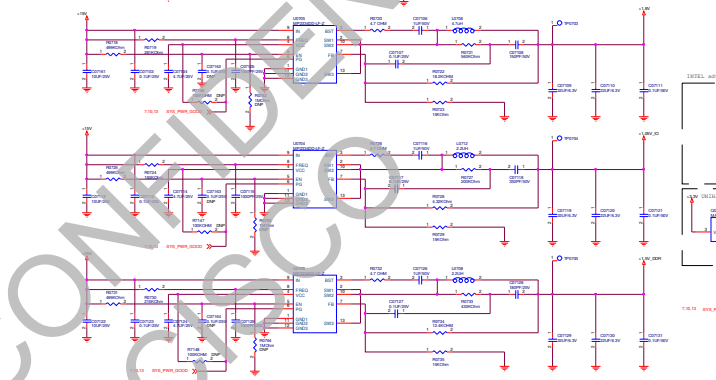
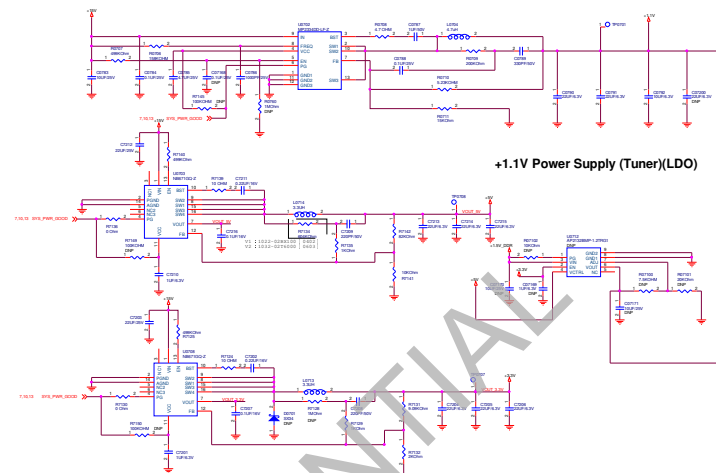
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14	PCIE INTERFACE
15	BBU SIMULATIONS
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18	XC1030(B)
19	XC1000-RF
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21	BSPG_DCX81
22	BOOT STRAPS
23	T1D OPTIONAL RESISTORS
24	TI BBU
25	DC Power Block Diagram
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Tyrik_Li
2012/12/28

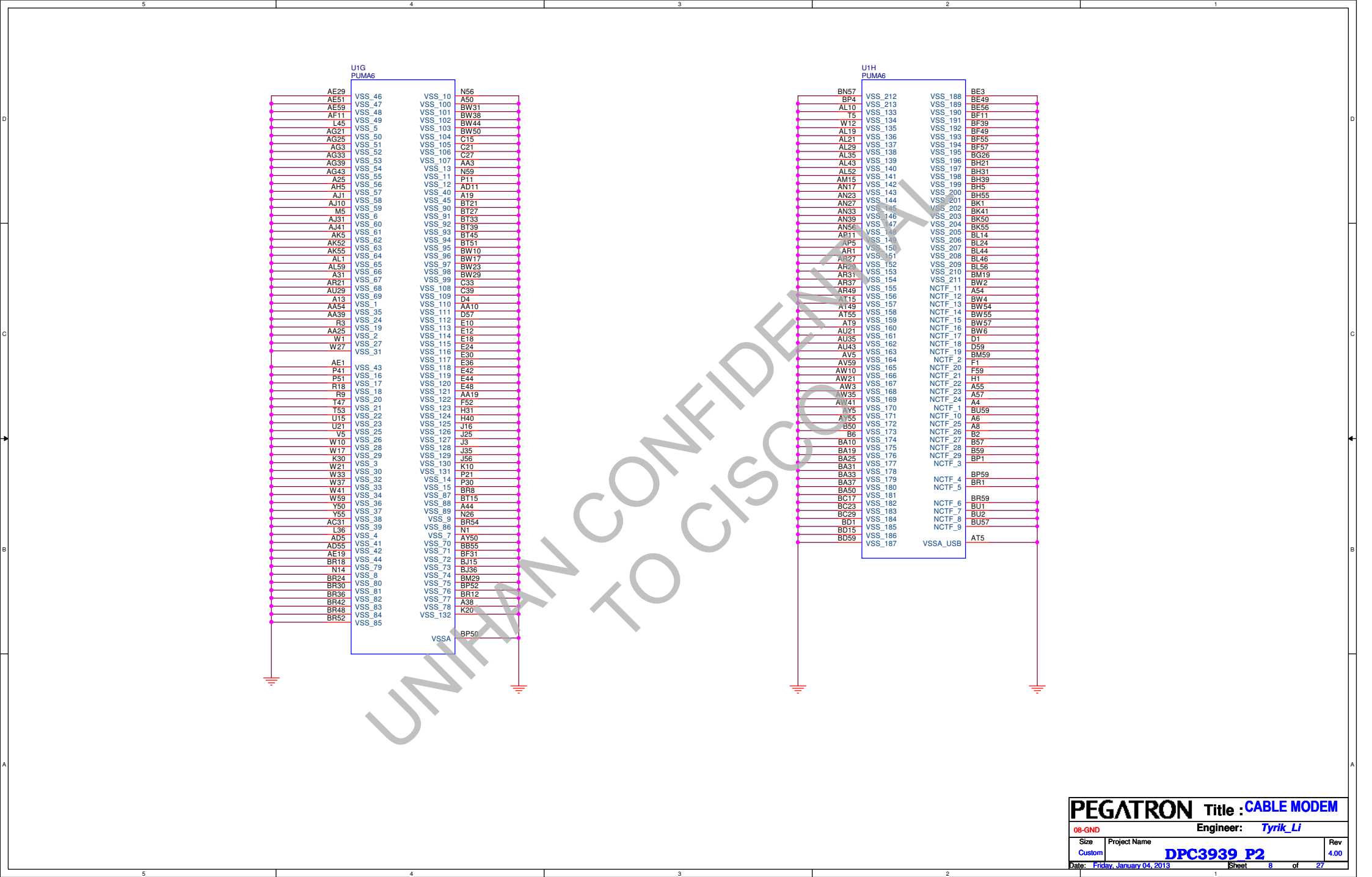


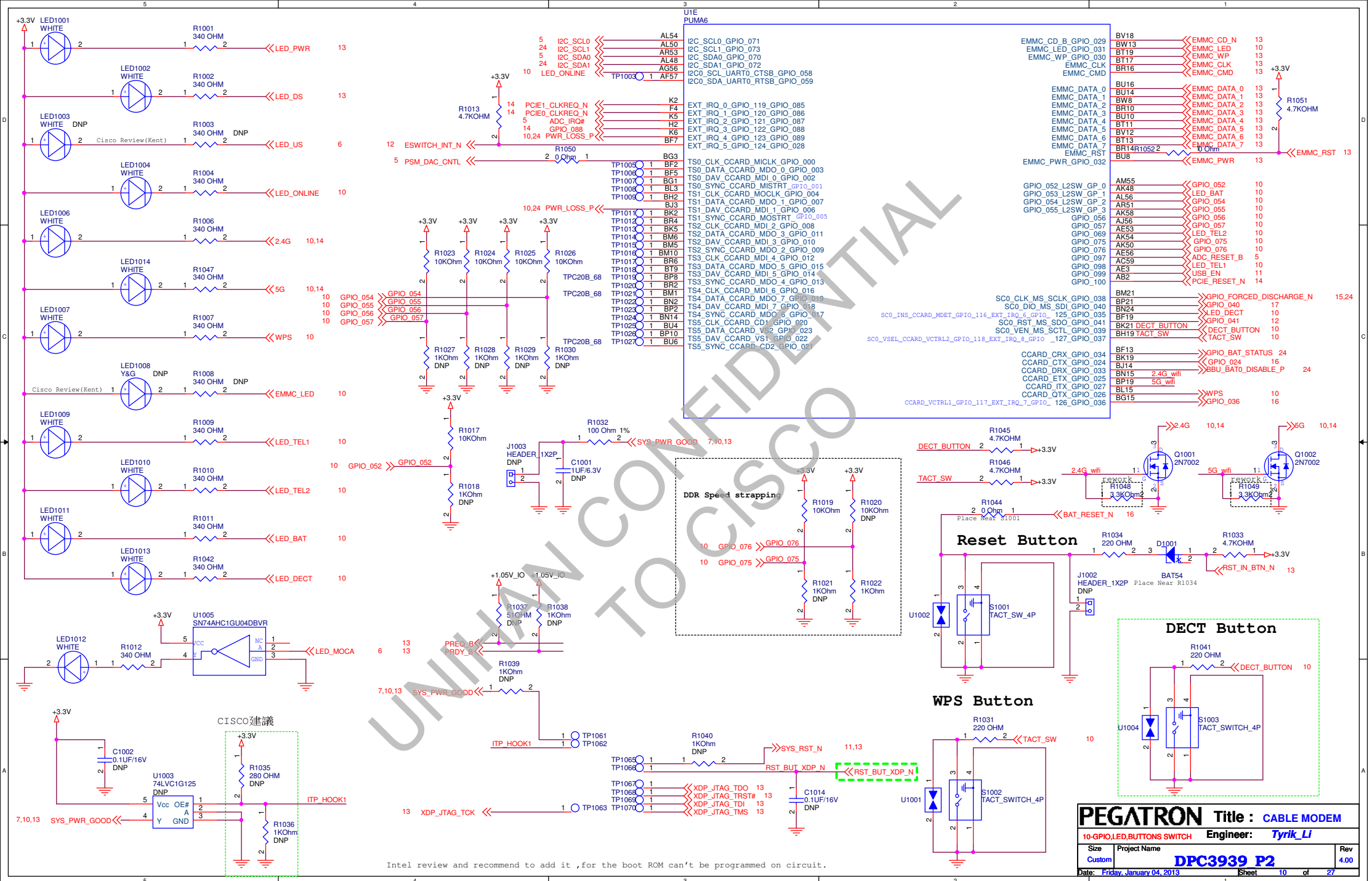




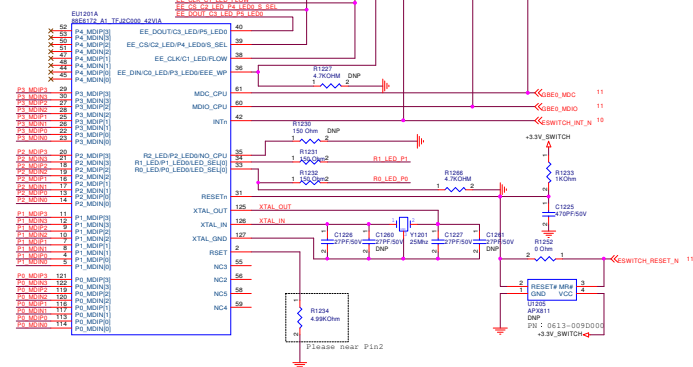
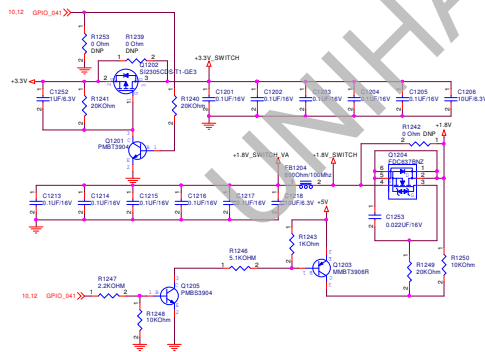
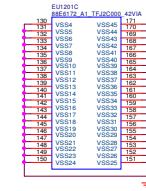
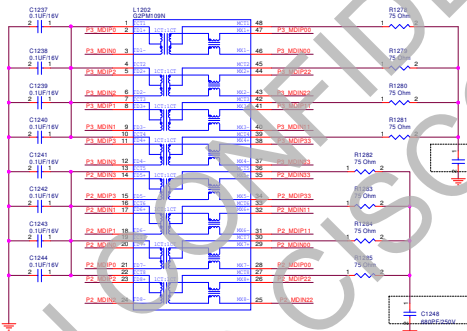
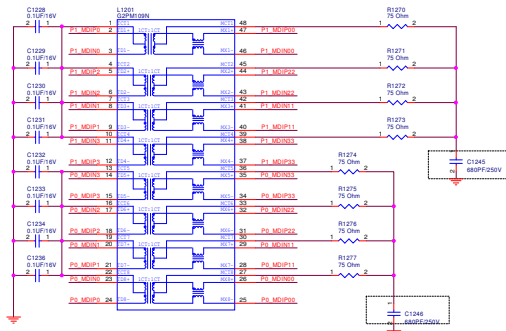
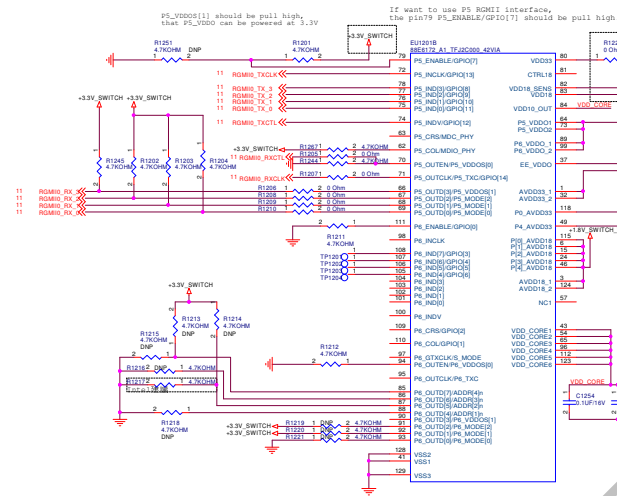
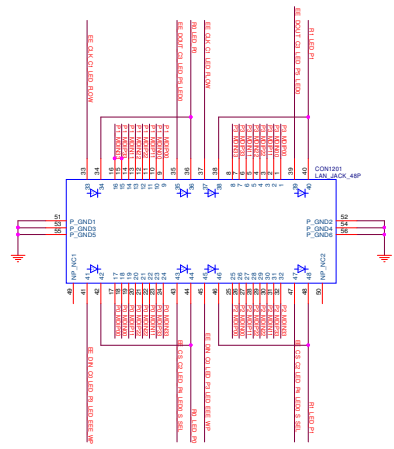


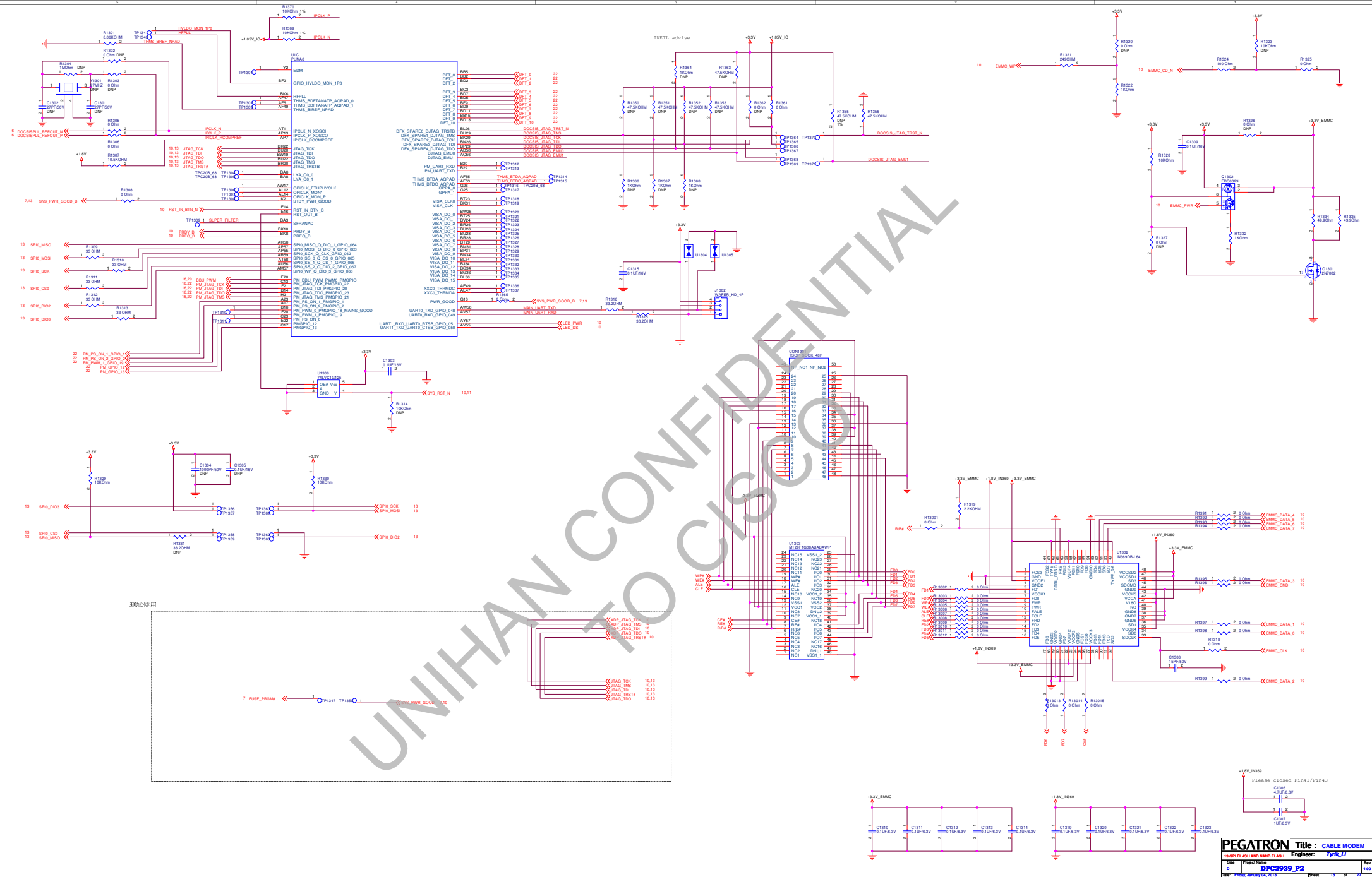
Vfb=0.6V	
R1=15KOHM	V_CORE=0.9V
R2A=30.1KOHM	V_CORE=0.95V
R2B=174KOHM	V_CORE=1.0V
R2C=86.6KOHM	V_CORE=1.05V

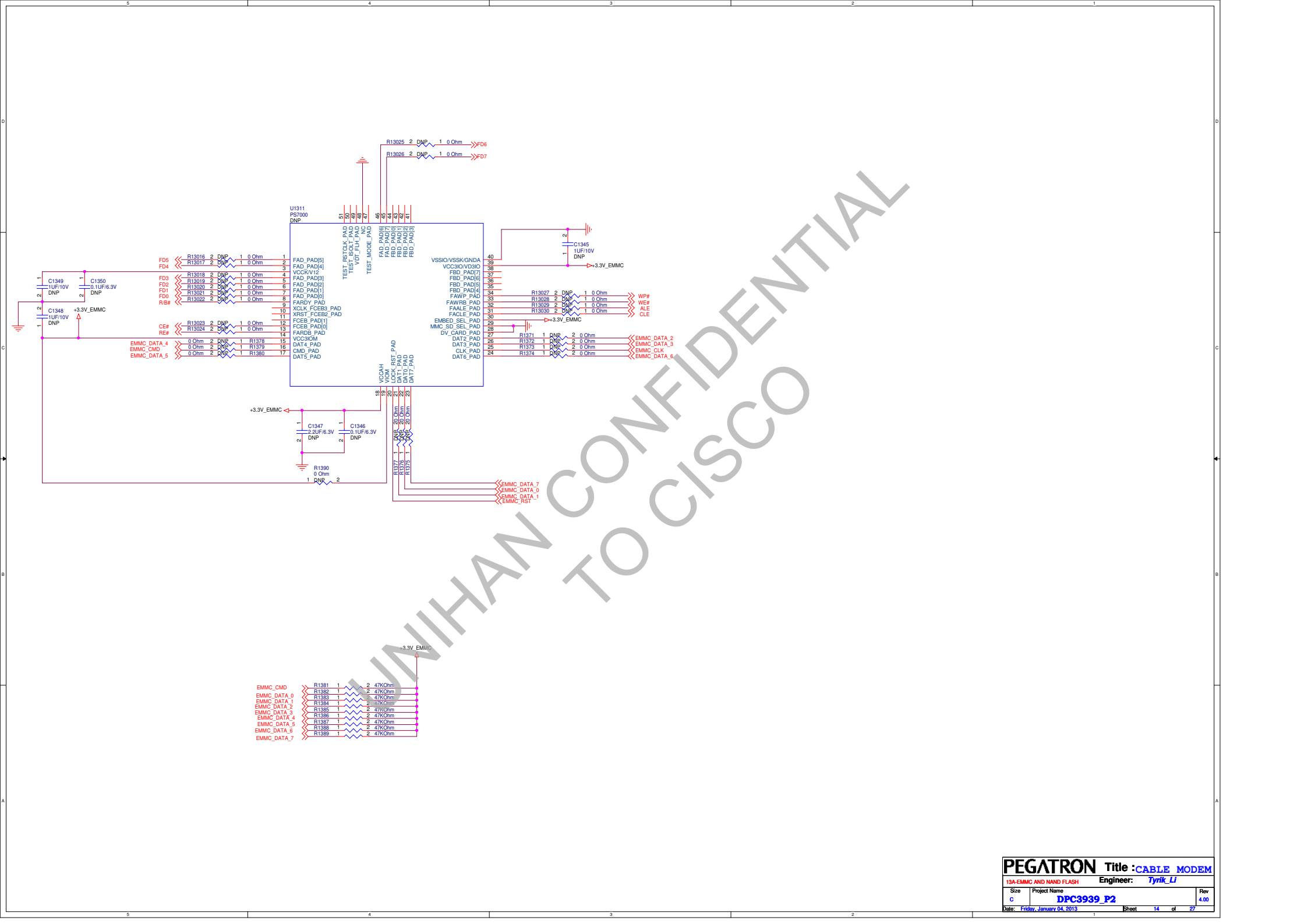


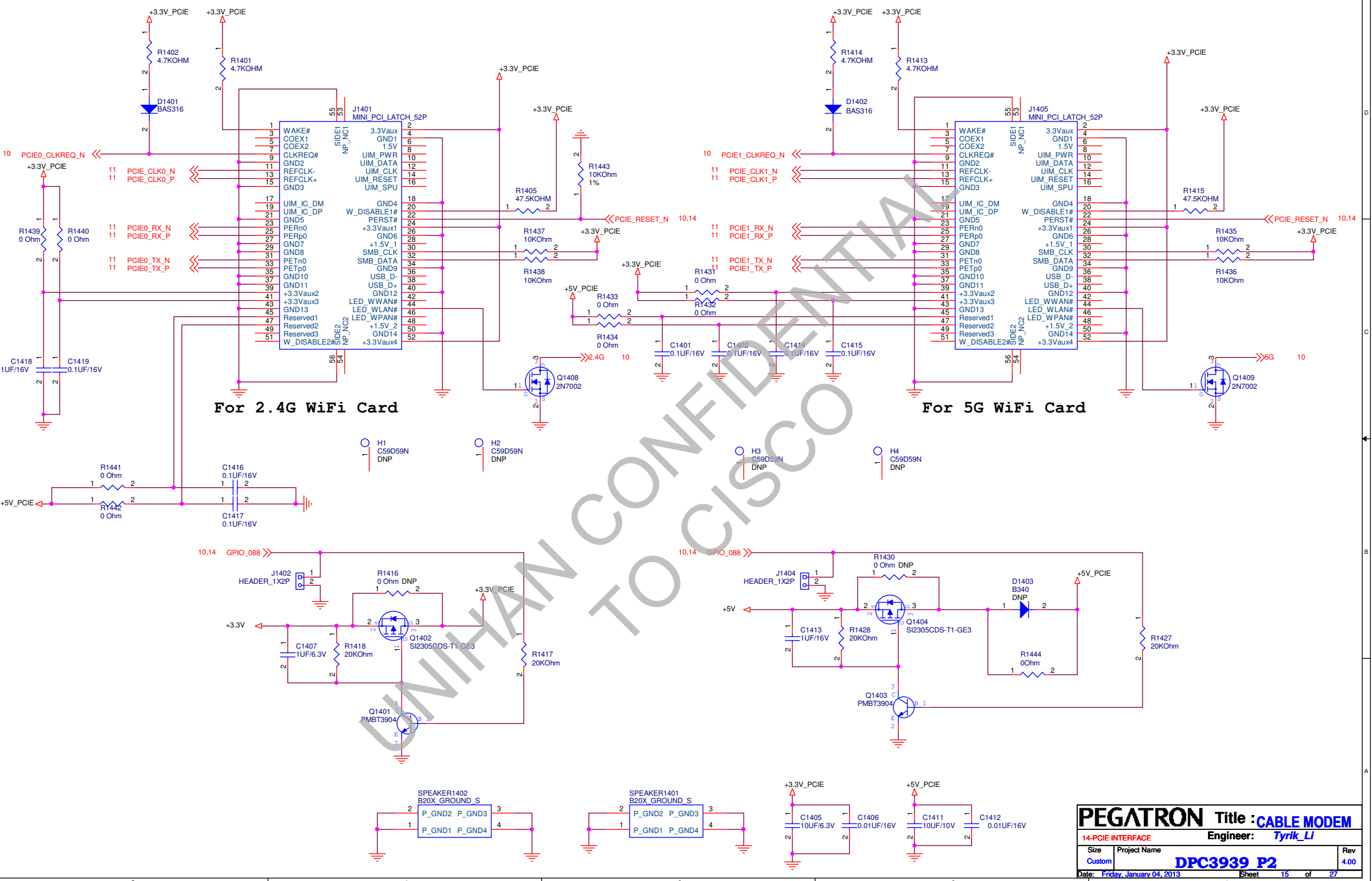


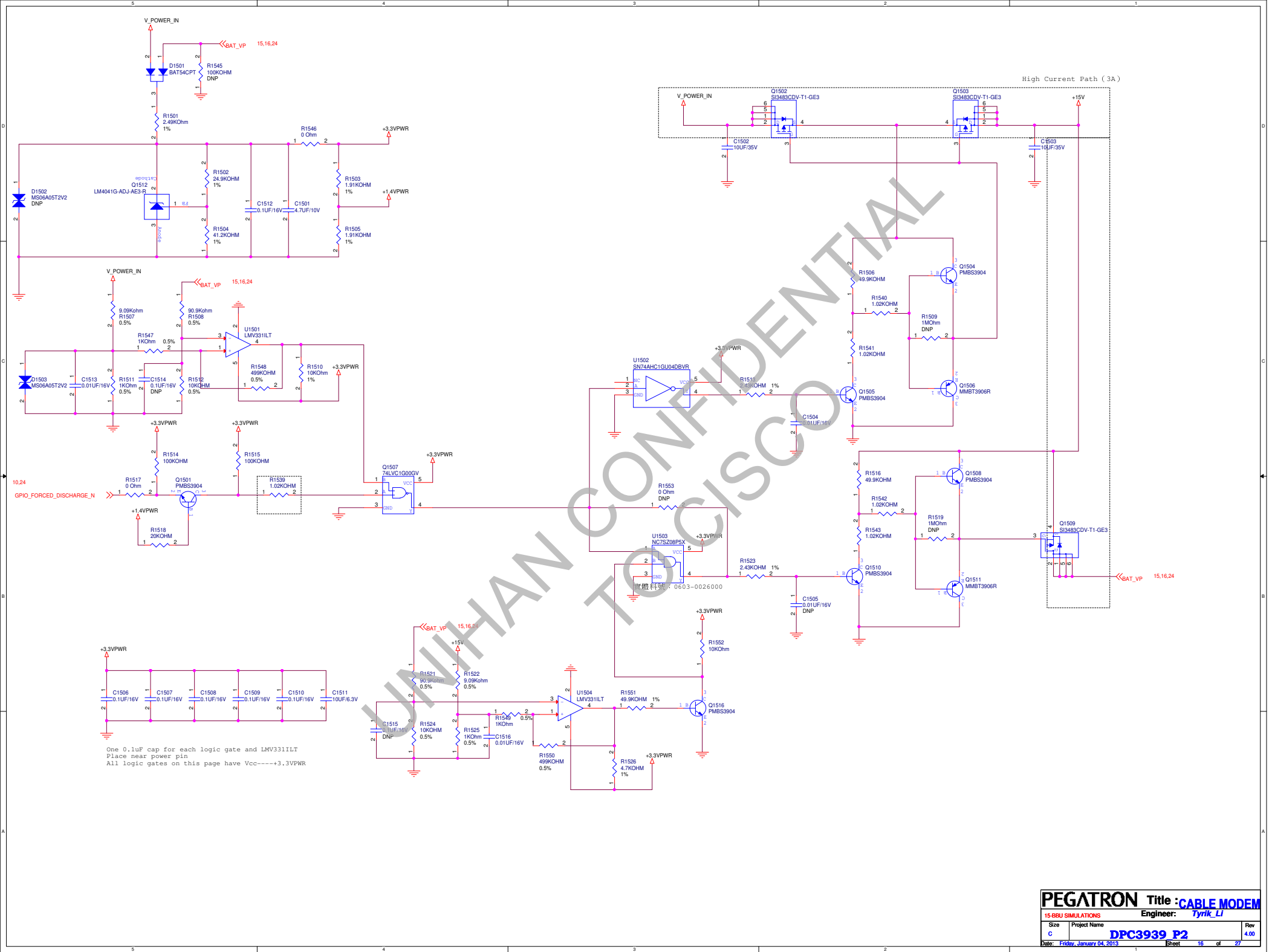
Intel review and recommend to add it ,for the boot ROM can't be programmed on circuit.



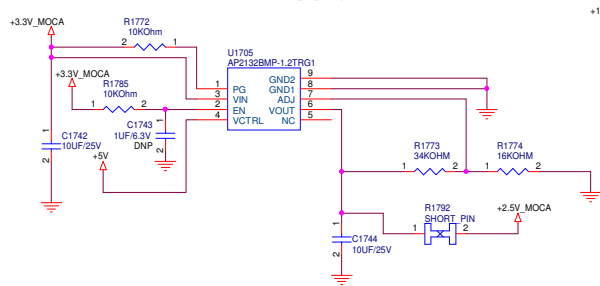




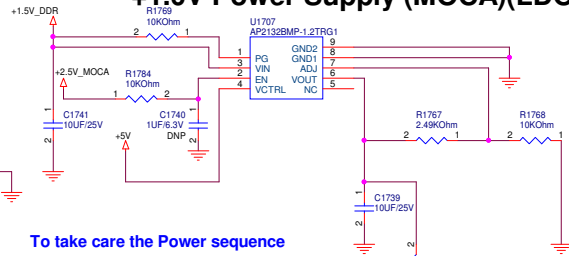




+2.5V Power Supply (MOCA)

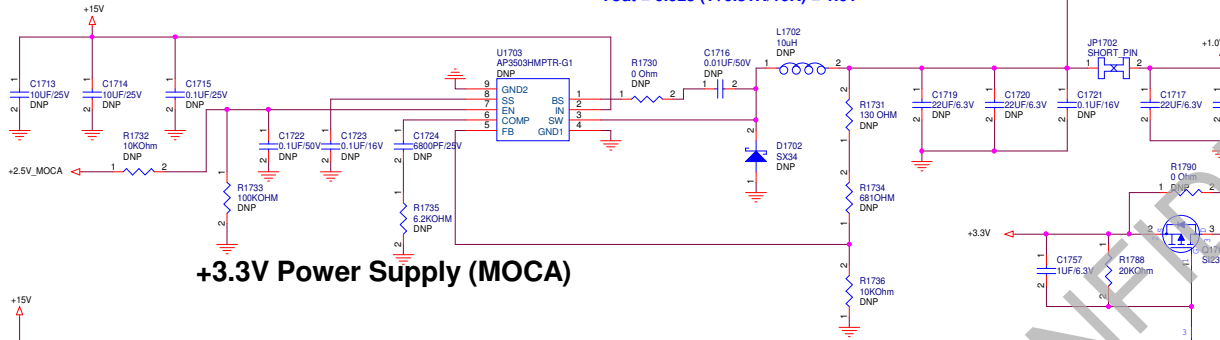


+1.0V Power Supply (MOCA)(LDO)



+1.0V Power Supply (MOCA)

default Vout = 1.0V
Vout = 0.925 (1+0.81K/10K) = 1.0V



+3.3V Power Supply (MOCA)

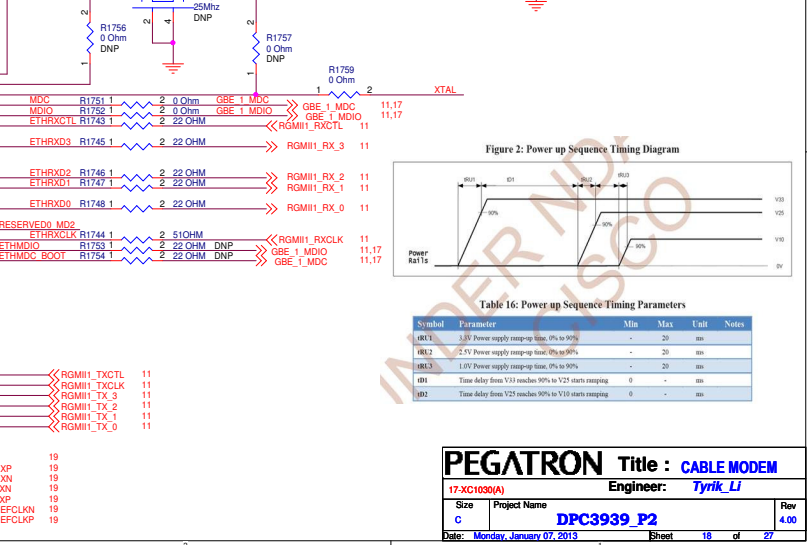
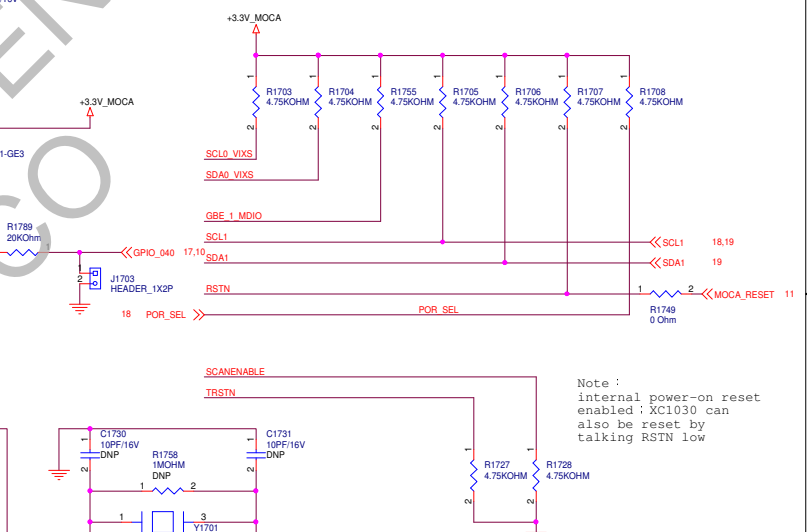
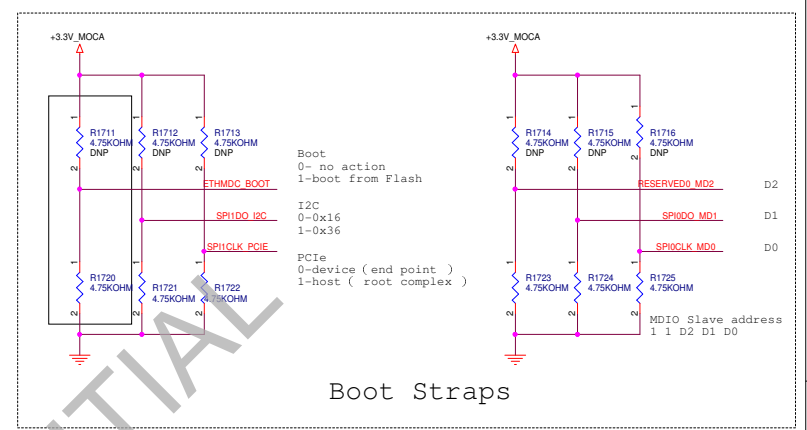
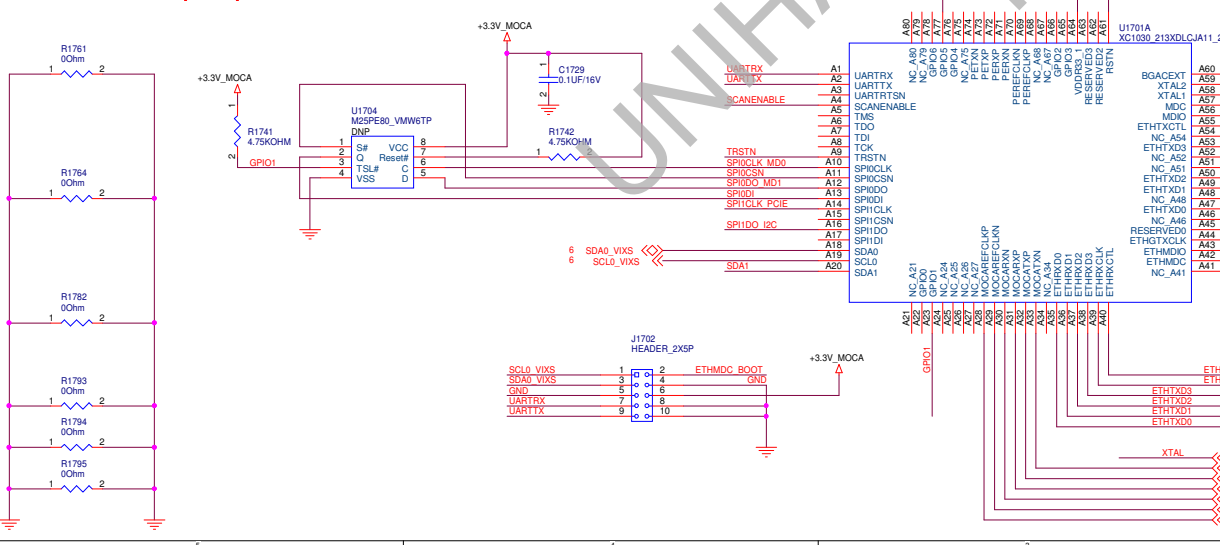
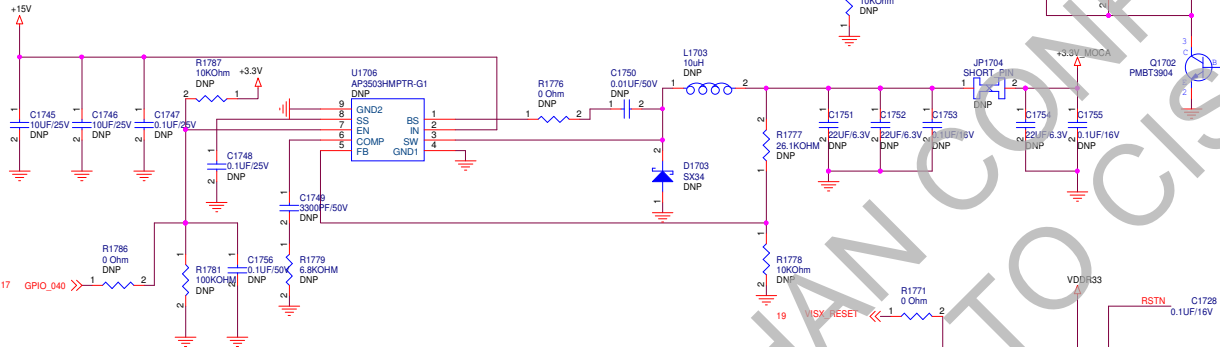


Figure 2: Power up Sequence Timing Diagram

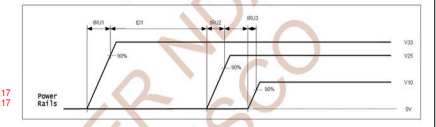
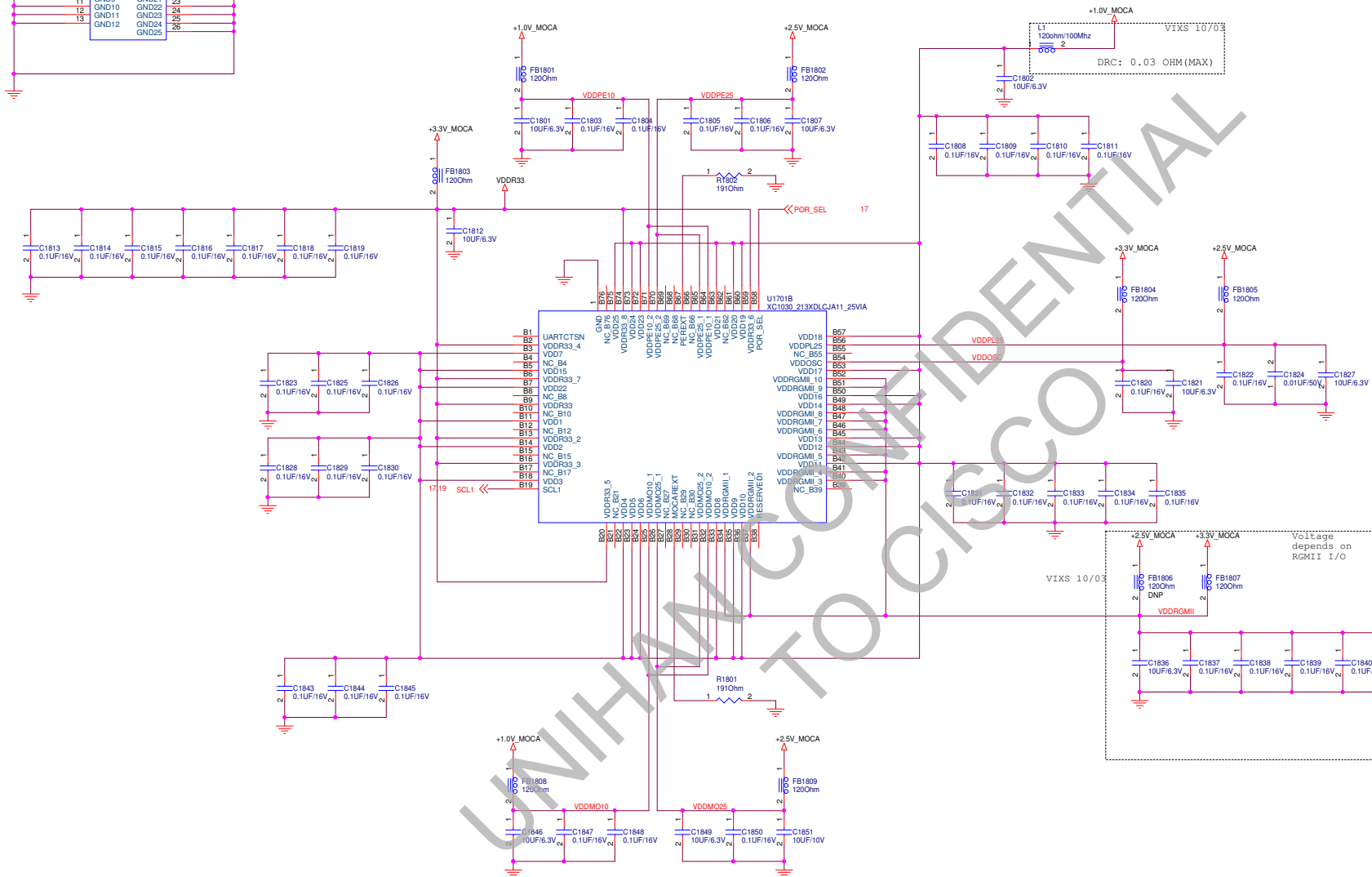
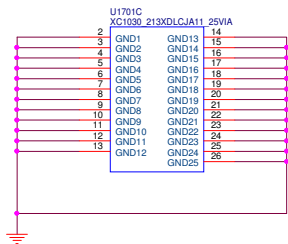
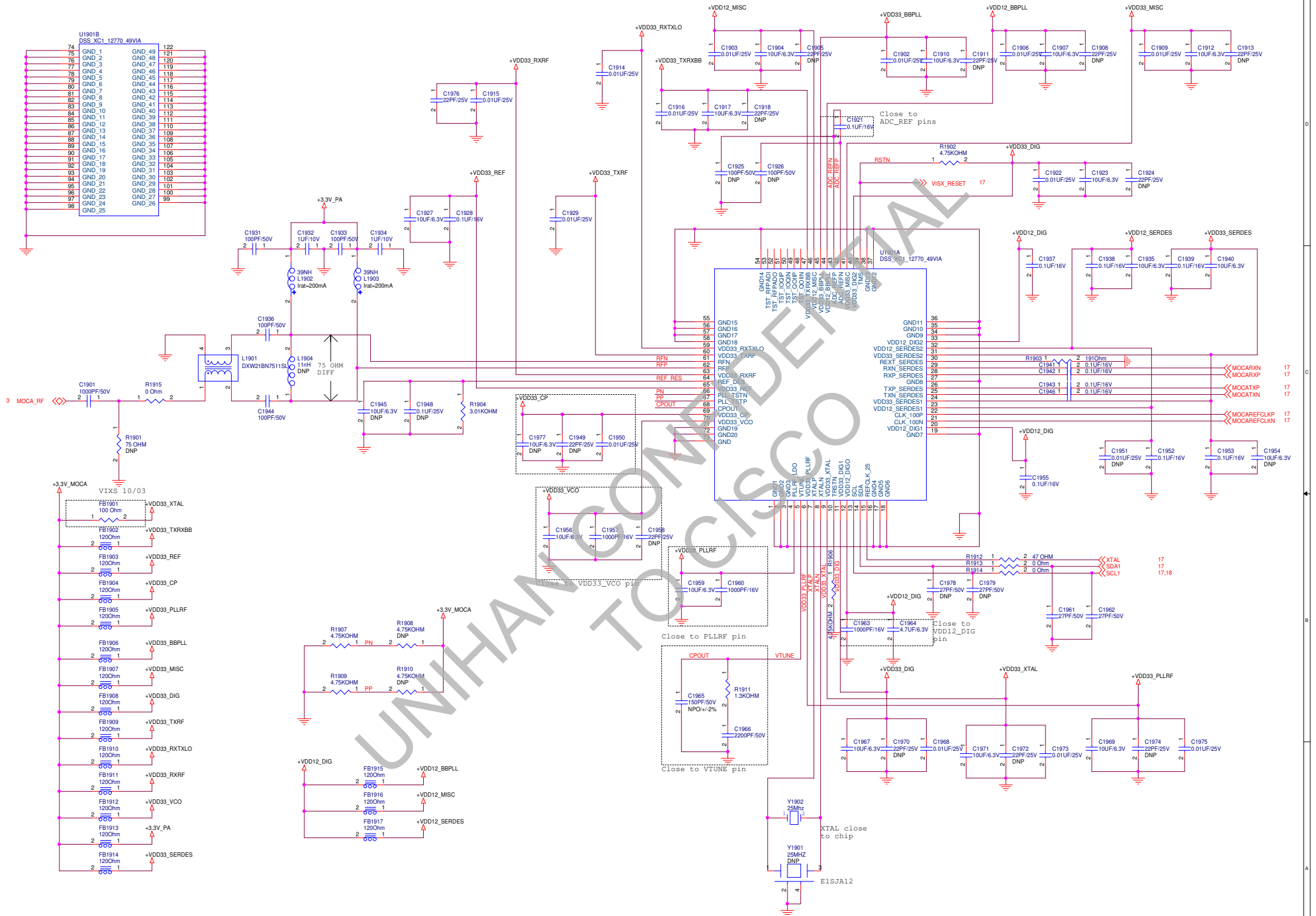
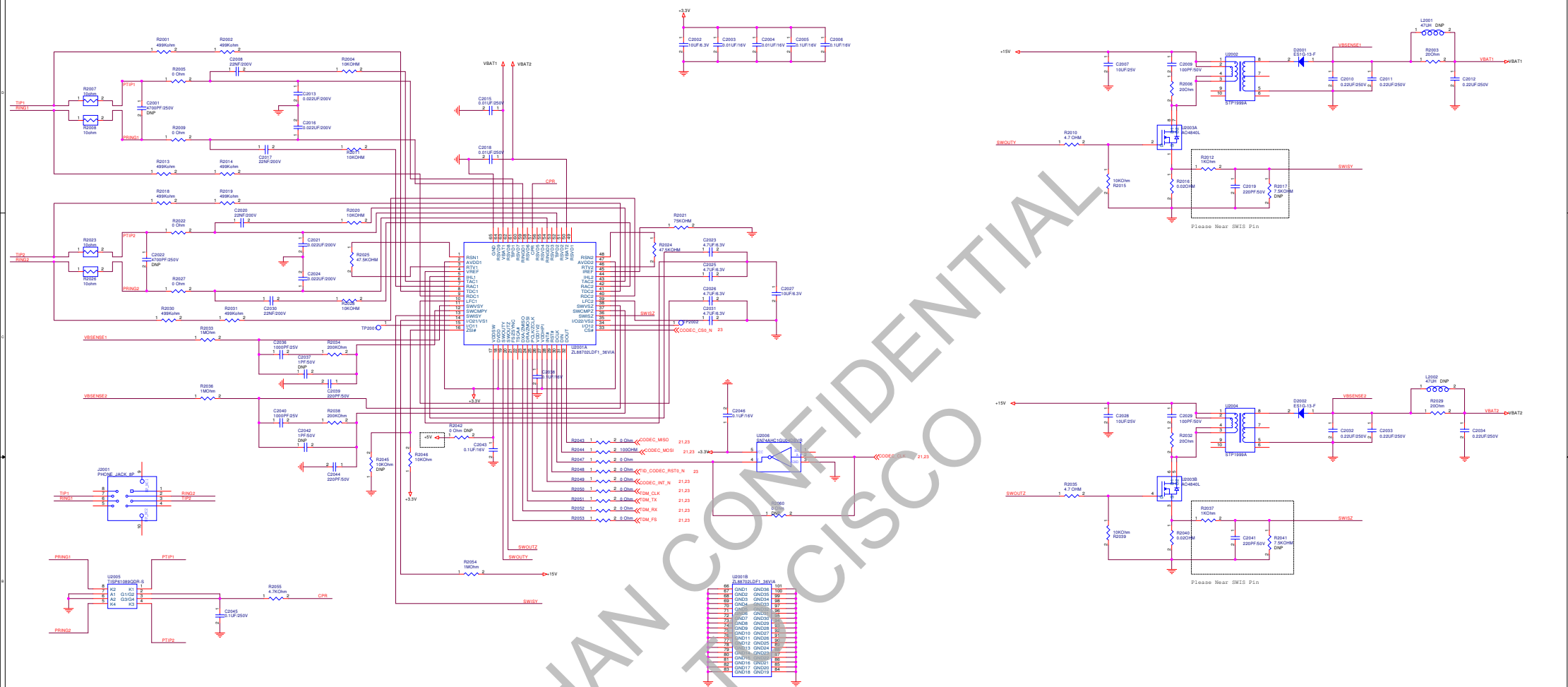


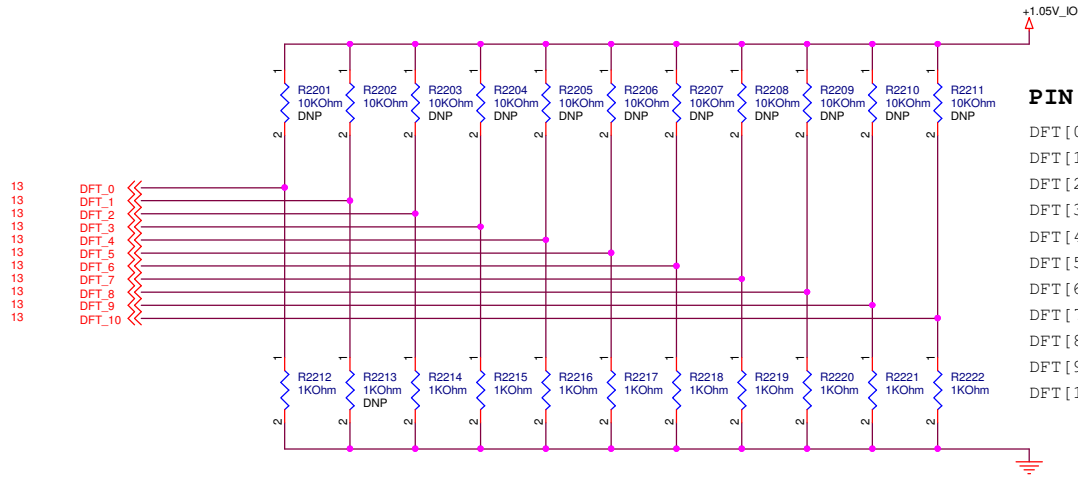
Table 16: Power up Sequence Timing Parameters

Symbol	Parameter	Min	Max	Unit	Notes
W1.1	3.3V Power supply ramp-up time, 0% to 90%	-	20	ms	
W1.2	2.5V Power supply ramp-up time, 0% to 90%	-	20	ms	
W1.3	1.0V Power supply ramp-up time, 0% to 90%	-	20	ms	
W2	Time delay from V33 reaches 90% to V25 starts ramping	0	-	ms	
W3	Time delay from V25 reaches 90% to V10 starts ramping	0	-	ms	

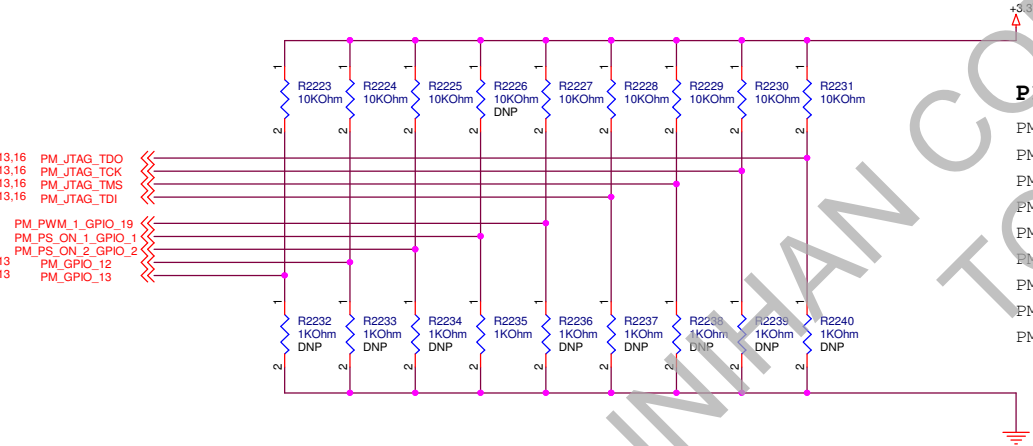




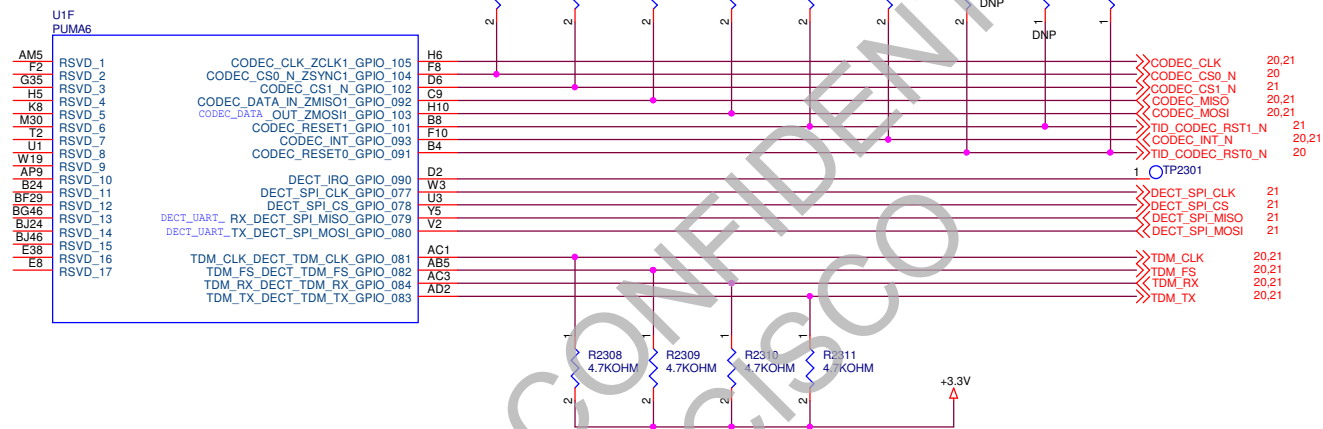




PIN NAME	STRAP NAME	DESCRIPTION
DFT[0]	SFR_VSRC_SEL	0: Use 1.8V
DFT[1]	BOOT_PATH[0]	01: EMMC
DFT[2]	BOOT_PATH[1]	
DFT[3]	ISCLK_BYP_STRAP	0: FPLL outputs are based on PLL output
DFT[4]	CLK_TEST_MODE	0: Clock test mode disabled
DFT[5]	FPLL_VALID_ALT	0: Design relies on valid signal from FPLL to proceed with power on
DFT[6]	Reserved	Reserved
DFT[7]	SEC_BOOT	0: Normal Boot
DFT[8]	Intel Manufacturing	0: Enable
DFT[9]	OEM Debug	0: Enable
DFT[10]	Reserved	Reserved

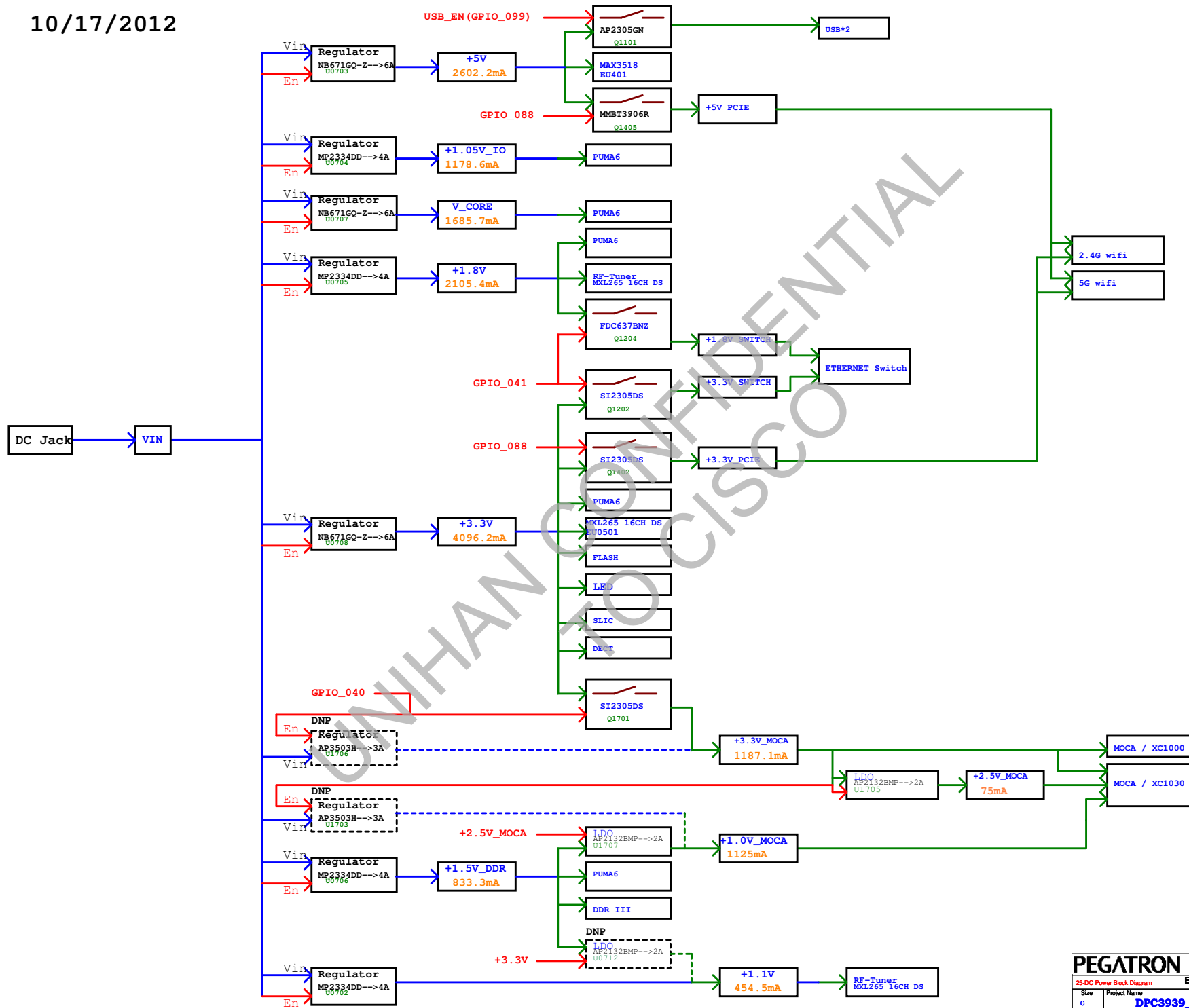


PIN NAME	STRAP NAME	DESCRIPTION
PM_JTAG_TDO_GPIO_23	RESET_OUT_SEL	1 = reset_outb is driven by HW
PM_JTAG_TCK_GPIO_22	PUNIT_DEBUG	1=Normal Operation
PM_JTAG_TMS_GPIO_21	FPLL_EXTCLK_FREQ_SEL	1=27 Mhz
PM_JTAG_TDI_GPIO_20	THRM_BYPASS	1=Firmware controls entry into FAIL_SAFE state
PM_PWM_1_GPIO_19	POSM_FAIL_SAFE	1=Normal Operation
PM_PS_ON_1_GPIO_1	FPLL_OSC_EN	1'b0: Bypass FPLL osc
PM_PS_ON_2_GPIO_2	FPLL_VRM_EN	1'b1: Enable FPLL VRM
PM_GPIO_12	POSM_BYPASS	1=Normal Operation
PM_GPIO_13	COLD_RESET_DISABLE	1=Cold reset results in warm reset



DPC3939 Power Architecture Phase II

10/17/2012



Item	Version	Description
1	DPC3939_P2 3.00	2012/11/22 1. Add U1310 and U1311 2. R1647,C1621 Populate 3. Remove the R303-R306 4. Add L0504,L0505 5. Swap L0503 Pin3 and Pin4 6. R2111,R2113 DNP 2012/11/27 1. R1044 change to 0 ohm 2. C1513,C1516 change to 0.01UF 3. R1671 change to 0 ohm 4. Add R1675,D1612 (DNP) 5. R1622 change to 4.99 ohm 6. Populate C1622 7. Remove Q2001,Q2002 8. C0505,C0506 change to 22pf 9. C305 change to 22pf L304 change to 0.18UH C308 change to 68pf 10.DECT RF modify 11.C305 change to 22pf L304 change to 0.18NH C307 change to 68pf 12. C0505,C0506 change to 22PF 2012/11/28 1. Remove U1310 DPC3939_P2 4.00 2012/12/24 1. TID_CODEC_RST0_N pull down 2. CODEC_CLK add U2006 3. R2044 change to 100 ohm 2012/12/26 1. TID_CODEC_RST0_N,TID_CODEC_RST1_N pull down 2. R2042 change to +5V 2012/12/28 1. C1121 change to 12PF 1. ADD C1122,C1124

Item	Version	Description
2	DPC3939_P2 1.00	2012/09/11 1. change ro MOCA 2.0 2. remove TI BBU 3. Murata diplexer design 4. remove two large capacitors in the SLIC 5. add 3.3K ohm between Pin land Pin 2 of Q1001,Q1002 6. C0547 chang to 22UF 7. R2125, R2126, R2127 to DNP Install R2212, R2122, R2123 8. U2107 DNP 9. R0616,R0617 DNP 10.change the BBU design 11.delete the +1.5V on PCIE 2012/09/12 1. RF shielding change to the design of DRG7908 2. add the net PSM_DAC_CNTL 3. populate R0614,R0615 DNP R0601,R0602 4. populate R0616,R0617 5. delete Q0201 6. delete R1141,R1142 7. IFCLK_P connect to +1.05V_IO through +10K ohm 8. populate R1658 9. add R1863 10. C2131,C2146 DNP 11. U2101 change to 0500-011M000 2012/09/14 1. C0547 change to 0.1UF,C0792 change to 10UF 2. C301 change to 100V then L301 3. delete C327,C328,R301,L317,L318 4. delete R0553,L0504,L0505 5. J1001 DNP 6. F1101,F1102 change to one fuse 1.5A 7. page 15,remove Battery Low Detect 8. Moca change to VIXS 9. Remove U2107 2012/09/21 1. MOCA VIXS change to the latest design 2. ETHMDC_BOOT connect to GBE_1_MDC ETHMDIO connect to GBE_1_MDIO 3. DNP R1101,R1102 4. C0798,C0799 change to SMT 5. delete R0413,R0415 6. R0416,R0417 change to 0402 size 7. add R1544 8. delete C0410 9. J1701 change to 0 ohm resister (DNP) 2012/09/27 1. Delete J1001,DNP U1003 2. Delete +5V_USB_B 3. DNP R1331,C1304,C1305 4. Change C1901 to 1000PF 50V 2012/10/03 1. Changed FB1901 to 100 Ohm and changed the name 2. Changed L1 to low DCR 2012/10/04 1. Modified XC1030/XC1000 symbol 2. add back TI BBU 2012/10/05 1. Modify BBU circuit
	DPC3939_P2 2.00	