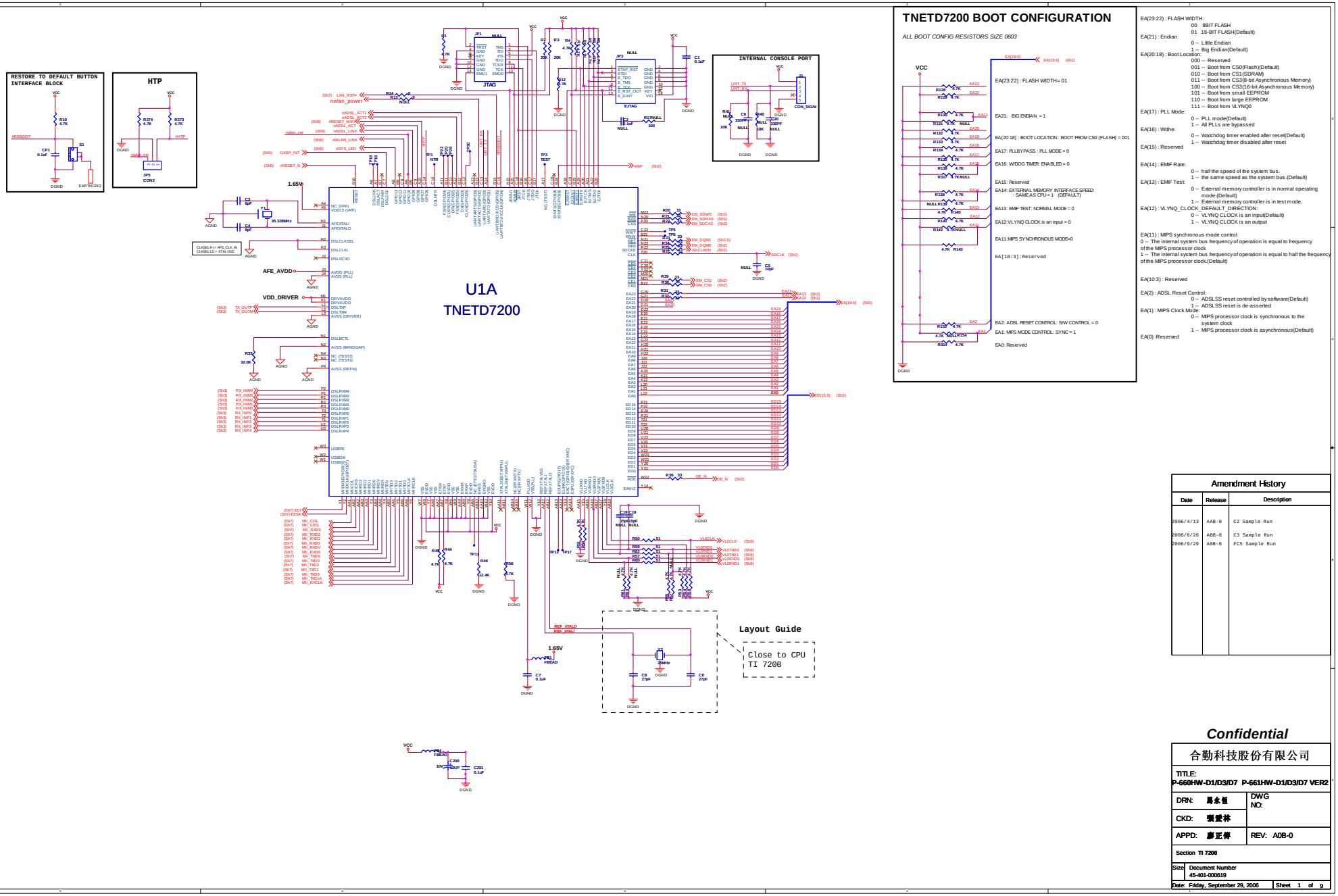

TNETD7200 BOOT CONFIGURATION

ALL BOOT CONFIG RESISTORS SIZE 0603

EA(23:22) : FLASH WIDTH= 01

EA21: BIG ENDIAN = 1

EA(20:18) : BOOT LOCATION : BOOT FROM CS0 (FLASH) = 001

EA17: PLLBYPASS : PLL MODE = 0

EA16: WIDOG TIMER: ENABLED = 0

EA15: Reserved

EA14: EXTERNAL MEMORY INTERFACE SPEED: : SAME AS CPU = 1 (DEFAULT)

EA13: EMIF TEST: NORMAL MODE = 0

EA12: VLYNQ CLOCK is an input = 0

EA11: MIPS SYNCHRONOUS MODE=0

EA[10:3]: Reserved

EA2: ADSL RESET CONTROL: S/W CONTROL = 0

EA1: MIPS MODE CONTROL: SYNC = 1

EA0: Reserved

EA(23:22) : FLASH WIDTH:
- 00 8BIT FLASH
- 01 16-BIT FLASH(Default)

EA(21) : Endian:
- 0 -- Little Endian
- 1 -- Big Endian(Default)

EA(20:18) : Boot Location:
- 000 -- Reserved
- 001 -- Boot from CS0(Flash)(Default)
- 010 -- Boot from CS1(SDRAM)
- 011 -- Boot from CS3(8-bit Asynchronous Memory)
- 100 -- Boot from CS3(16-bit Asynchronous Memory)
- 101 -- Boot from small EEPROM
- 110 -- Boot from large EEPROM
- 111 -- Boot from VLYNQ0

EA(17) : PLL Mode:
- 0 -- PLL mode(Default)
- 1 -- All PLLs are bypassed

EA(16) : Widhe:
- 0 -- Watchdog timer enabled after reset(Default)
- 1 -- Watchdog timer disabled after reset

EA(15) : Reserved

EA(14) : EMIF Rate:
- 0 -- half the speed of the system bus.
- 1 -- the same speed as the system bus.(Default)

EA(13) : EMIF Test:
- 0 -- External memory controller is in normal operating mode.(Default)
- 1 -- External memory controller is in test mode.

EA(12) : VLYNQ_CLOCK_DEFAULT_DIRECTION:
- 0 -- VLYNQ CLOCK is an input(Default)
- 1 -- VLYNQ CLOCK is an output

EA(11) : MIPS synchronous mode control:
0 -- The internal system bus frequency of operation is equal to frequency of the MIPS processor clock
1 -- The internal system bus frequency of operation is equal to half the frequency of the MIPS processor clock.(Default)

EA(10:3) : Reserved

EA(2) : ADSL Reset Control:
- 0 -- ADSLSS reset controlled by software(Default)
- 1 -- ADSLSS reset is de-asserted

EA(1) : MIPS Clock Mode:
- 0 -- MIPS processor clock is synchronous to the system clock
- 1 -- MIPS processor clock is asynchronous(Default)

EA(0) :Reserved

Amendment History

Date	Release	Description
2006/4/13	AAB-0	C2 Sample Run
2006/6/26	ABB-0	C3 Sample Run
2006/9/29	ABB-0	FCS Sample Run

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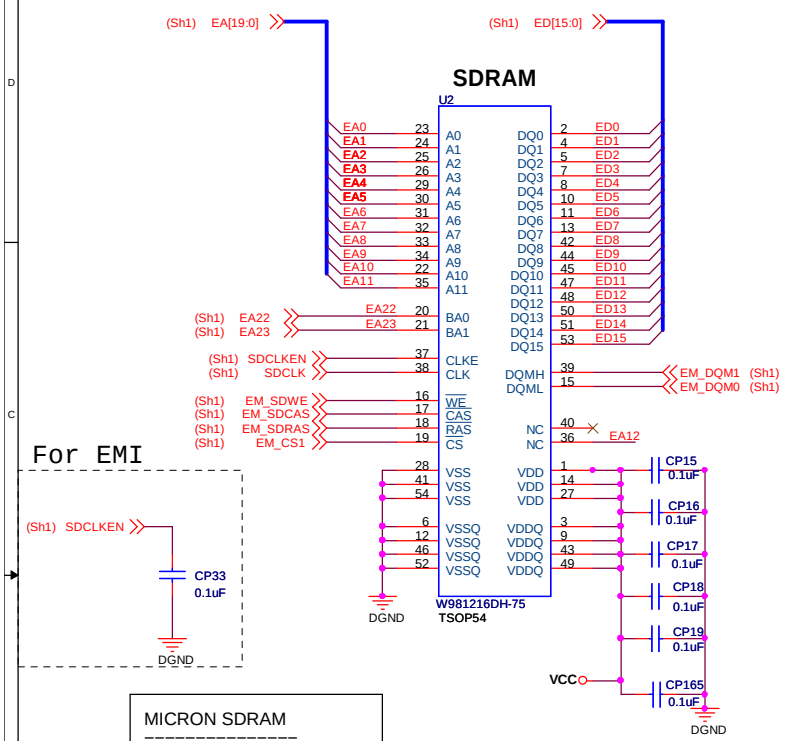
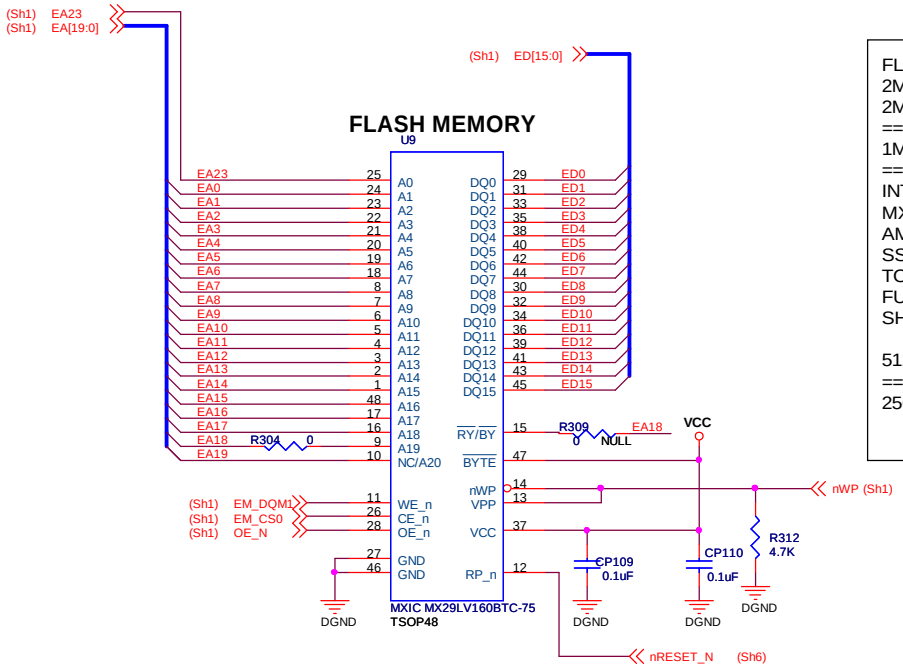
TITLE: P-660HW-D1/D3/D7 P-661HW-D1/D3/D7 VER2

DRN: 易永恒	DWG NO:
CKD: 張愛林	
APPD: 廖正得	REV: A0B-0
Section TI 7200	
Size: Document Number 45-401-000619	
Date: Friday, September 29, 2006	Sheet 1 of 9



For EMI

MICRON SDRAM
==========
8Mx16 => MT48LC8M16A2
Winbond W981216DH-75
ETRON EM639165TS-7.5
OR
16Mx16=>
Winbond W982516CH



FLASH MEMORY
2MX16 : MXIC MX29LV320BTC-75
2MX16 : AMD AM29LV320D
======
1MX16
======
INTEL TE28F160C3BD70
MXIC 29LV160BTC-75
AMD AM29LV160DB-120EC
SST SST39VF160-90-4C-EK
TOSHIBA TC58FVB160FT-12
FUJITSU MBM29LV160BE-12
SHARP LH28F160BJE-BTL90

512KX16 : AMD AM29LV800
=======
256KX16 : MX29LV400BTC-90
EN29LV400B

```
---Flash  define---
A17 : 4M Bits
A18 : 8M Bits
A19 : 16M Bits
A20 : 32M Bits
A21 : 64M Bits
```

	AMD	INTEL
R304	0	NULL
R309	NULL	0

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TITLE:
P-660HW-D1/D3/D7 P-661HW-D1/D3/D7 VER2

DRN: 馬永恆	DWG NO:
CKD: 張愛林	
APPD: 廖正傳	REV: A0B-0

Section **flash&sdram**

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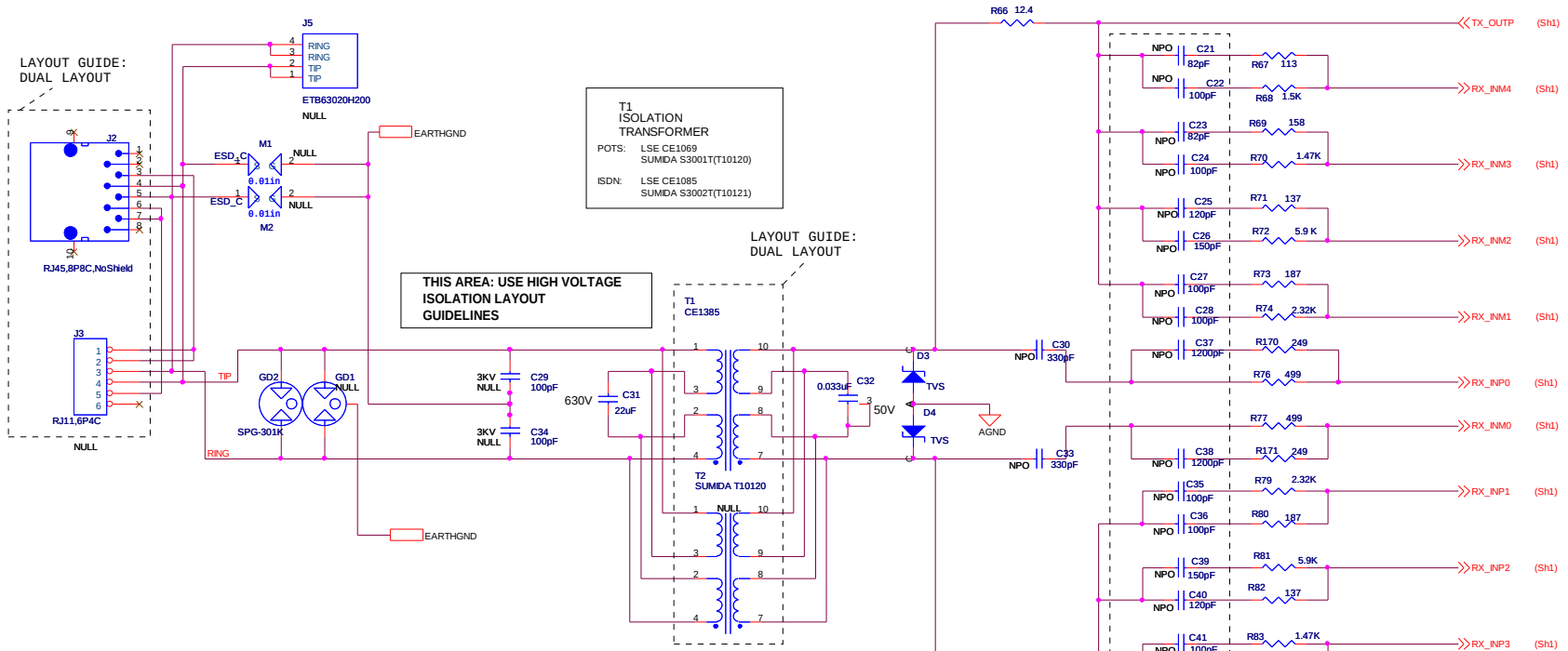

For P-660HW-D1 & P-660HW-D3 populate values as follows:

Components	P-660HW-D1(Annex_A)	P-660HW-D3(Annex_B)
R74,R79	232 ohm	1.18K ohm
C28,C35	180pF	220pF
R73,R80	3.32K ohm	196K ohm
C27,C36	270pF	56pF
R72,R81	158ohm	1.1K
C26,C39	180pF	220PF
R71,R82	6.49K ohm	NULL
C25,C40	330pF	NULL
R70,R83	499 ohm	NULL
C24,C41	220pF	Null
R69,R84	4.99K ohm	Null
C23,C42	270pF	Null
R68,R85	158 ohm	Null
C22,C43	180pF	Null
R67,R86	4.02K	Null
C21,C44	470pF	Null
R171,R170	249 ohm	Null
C37,C38	390pF	Null
C31	0.033uF	0.022uF
C30,C33	680pF	330pF
T1	CE1069	CE1085
C32	1uF	0.033uF

Note : NPO Material

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TITLE:
P-660HW-D1/D3/D7 P-661HW-D1/D3/D7 VER2

DRN: 馬永恆	DWG NO:
CKD:張愛林	
APPD: 廖正傳	REV: A0B-0

Section **ADSL HYBRID**

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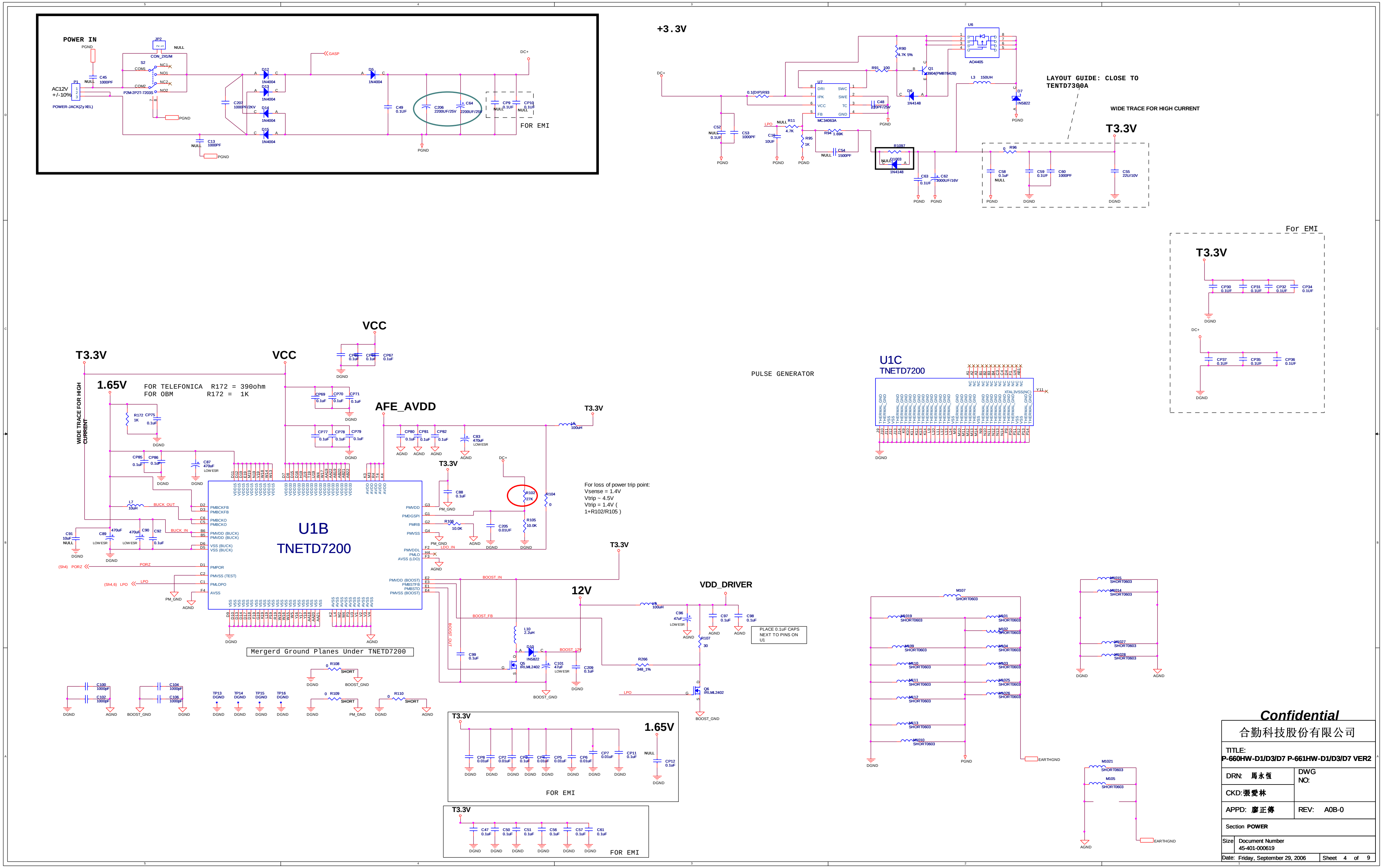
POWER IN
AC12V +/-10%
POWER-JACK(Zy XEL)
FOR EMI
+3.3V
LAYOUT GUIDE: CLOSE TO TENTD7300A
WIDE TRACE FOR HIGH CURRENT
T3.3V
For EMI
VCC
PULSE GENERATOR
U1C
TNETD7200
1.65V
FOR TELEFONICA R172 = 390ohm
FOR OBM R172 = 1K
WIDE TRACE FOR HIGH CURRENT
AFE_AVDD
U1B
TNETD7200
For loss of power trip point:
Vsense = 1.4V
Vtrip = 4.5V
Vtrip = 1.4V (1+R102/R105)
12V
VDD_DRIVER
PLACE 0.1uF CAPS NEXT TO PINS ON U1
Mergerd Ground Planes Under TNETD7200
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TITLE: P-660HW-D1/D3/D7 P-661HW-D1/D3/D7 VER2
DRN: 周永恒
DWG NO:
CKD: 張愛林
APPD: 廖正偉
REV: A0B-0
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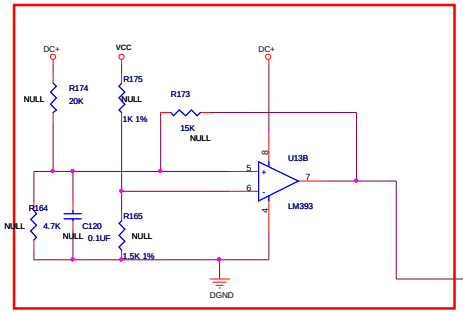
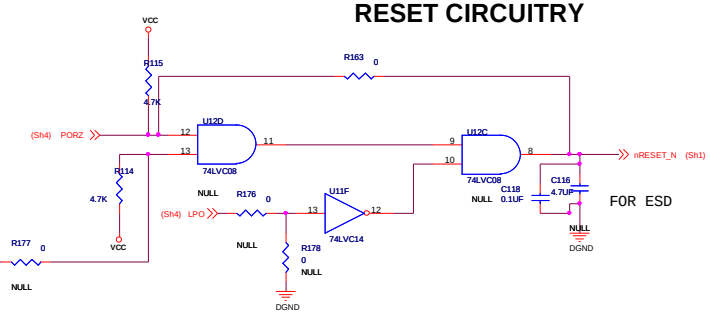
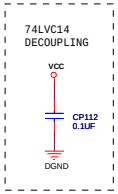
REGENERATIVE COMPARATOR CIRCUITRY

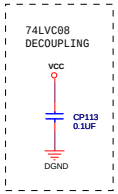


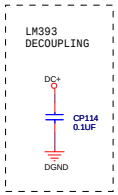
RESET CIRCUITRY



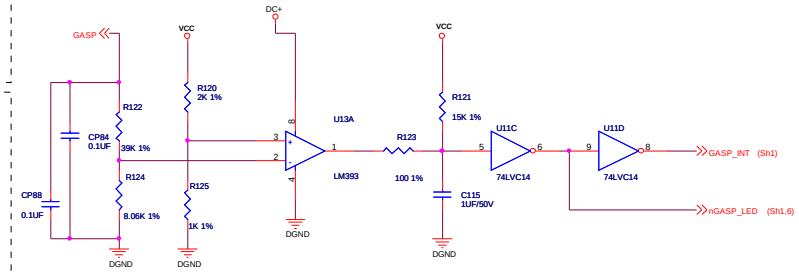
FOR ESD







DYING GASP CIRCUITRY



	for telefonica	not for telefonica
R174	20K 1%	NULL
R175	1K 1%	NULL
R165	1.5K 1%	NULL
R164	4.7K1%	NULL
R173	15K 1%	NULL
C120	NULL	NULL
R163	NULL	0
R176	0	NULL
C116	4.7UF	NULL
C118	NULL	0.1UF
R177	0	NULL
R122	39K	56K
U12	74LVC08	NULL

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TITLE: P-660HW-D1/D3/D7 P-661HW-D1/D3/D7 VER2	
DRN: 扈永恒	DWG NO:
CKD: 張愛林	
APPD: 廖正傳	REV: A0B-0
Section RESET & DYING GASP	
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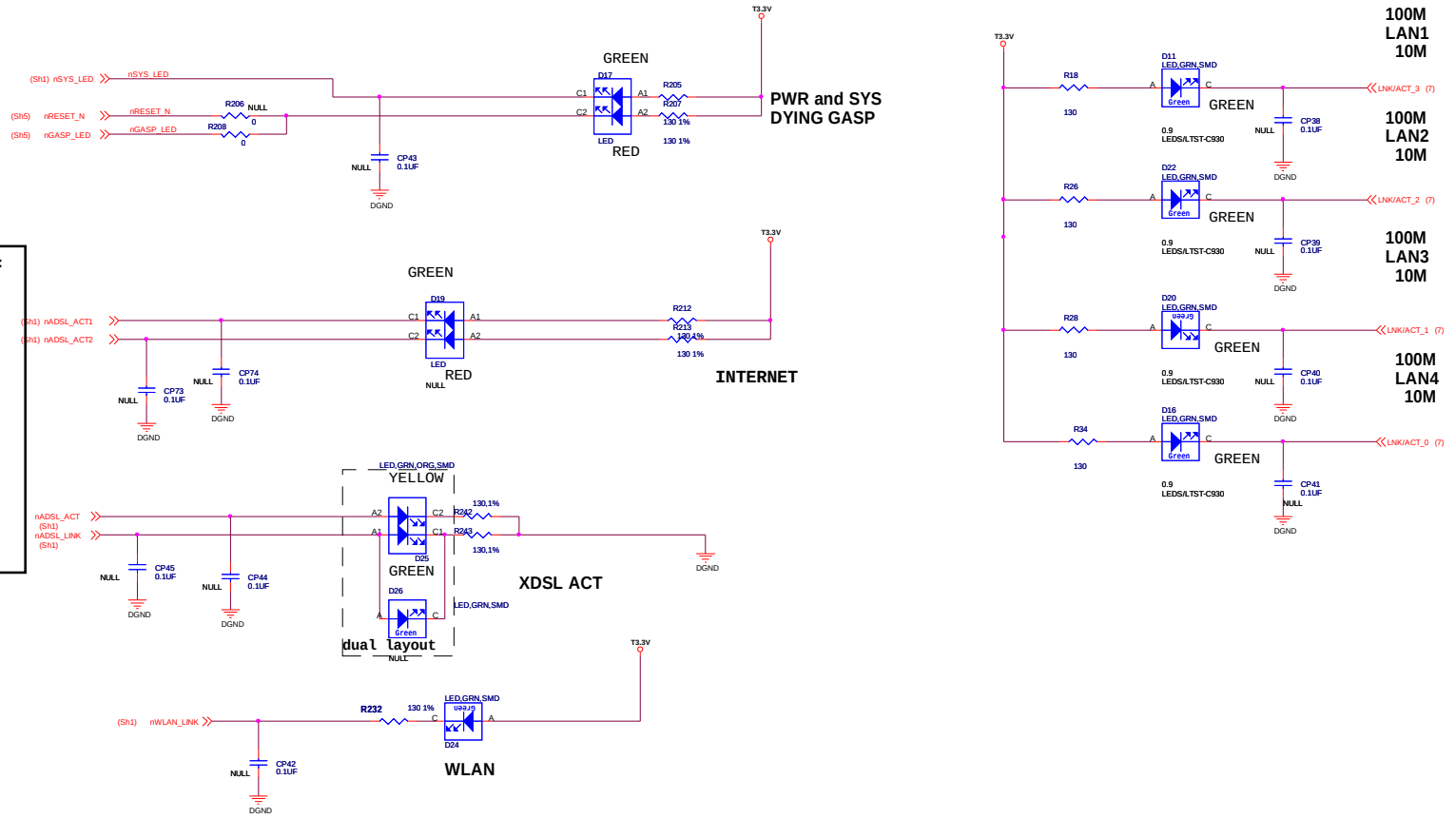

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CKD: 張愛林	
APPD: 廖正傳	REV: A0B-0
Section LED DISPLAY	
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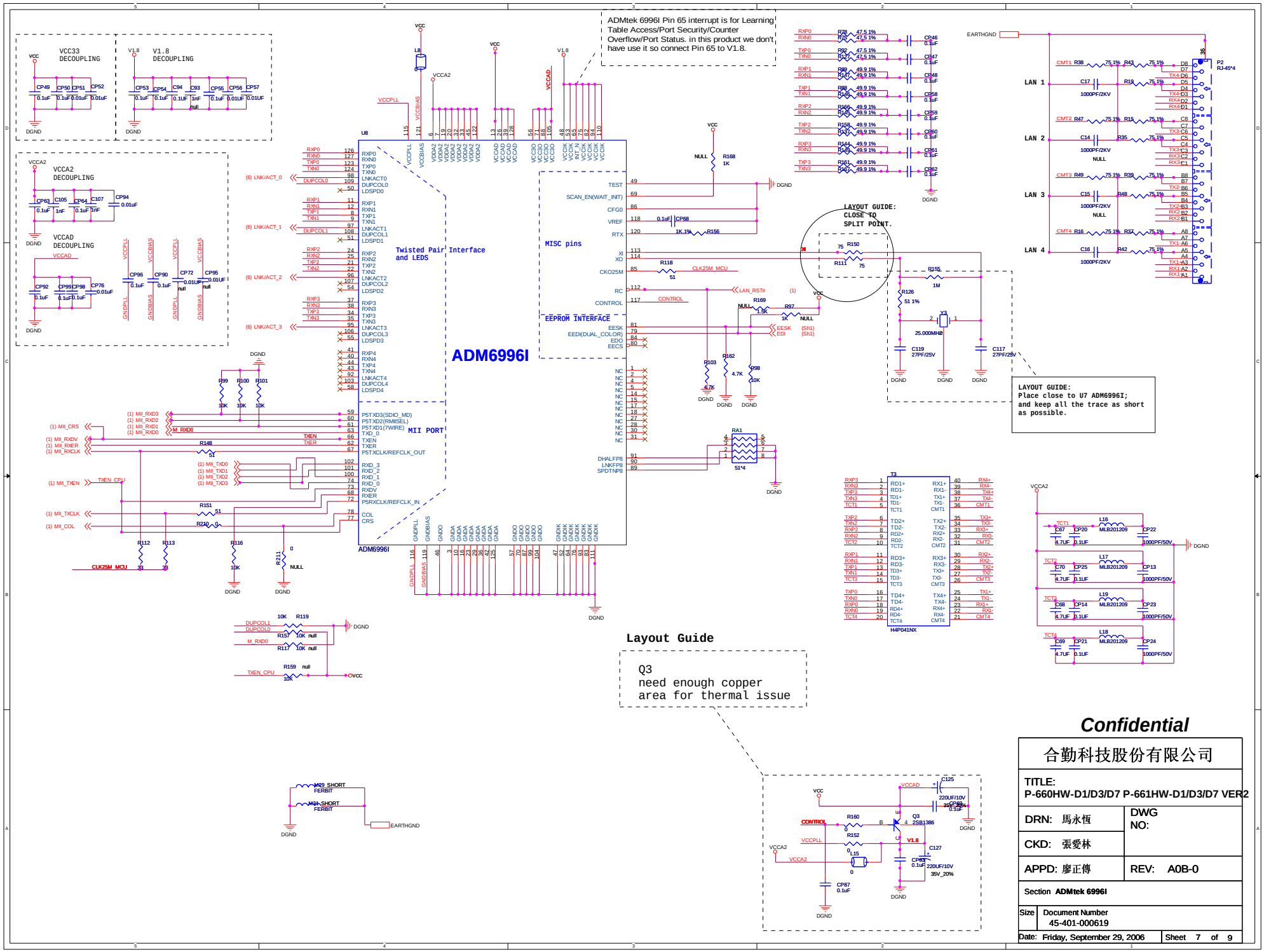
ADMtek 6996I Pin 65 interrupt is for Learning Table Access/Port Security/Counter Overflow/Port Status. in this product we don't have use it so connect Pin 65 to V1.8.
VCC33 DECOUPLING
V1.8 DECOUPLING
VCCA2 DECOUPLING
VCCAD DECOUPLING
ADM6996I
Twisted Pair Interface and LEDS
MII PORT
MISC pins
EEPROM INTERFACE
LAYOUT GUIDE: CLOSE TO SPLIT POINT.
LAYOUT GUIDE: Place close to U7 ADM6996I; and keep all the trace as short as possible.
Layout Guide
Q3 need enough copper area for thermal issue
LAN 1
LAN 2
LAN 3
LAN 4
H4P041NX
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TITLE: P-660HW-D1/D3/D7 P-661HW-D1/D3/D7 VER2
DRN: 馬永恆
CKD: 張愛林
APPD: 廖正傳
DWG NO:
REV: A0B-0
Section ADMtek 6996I
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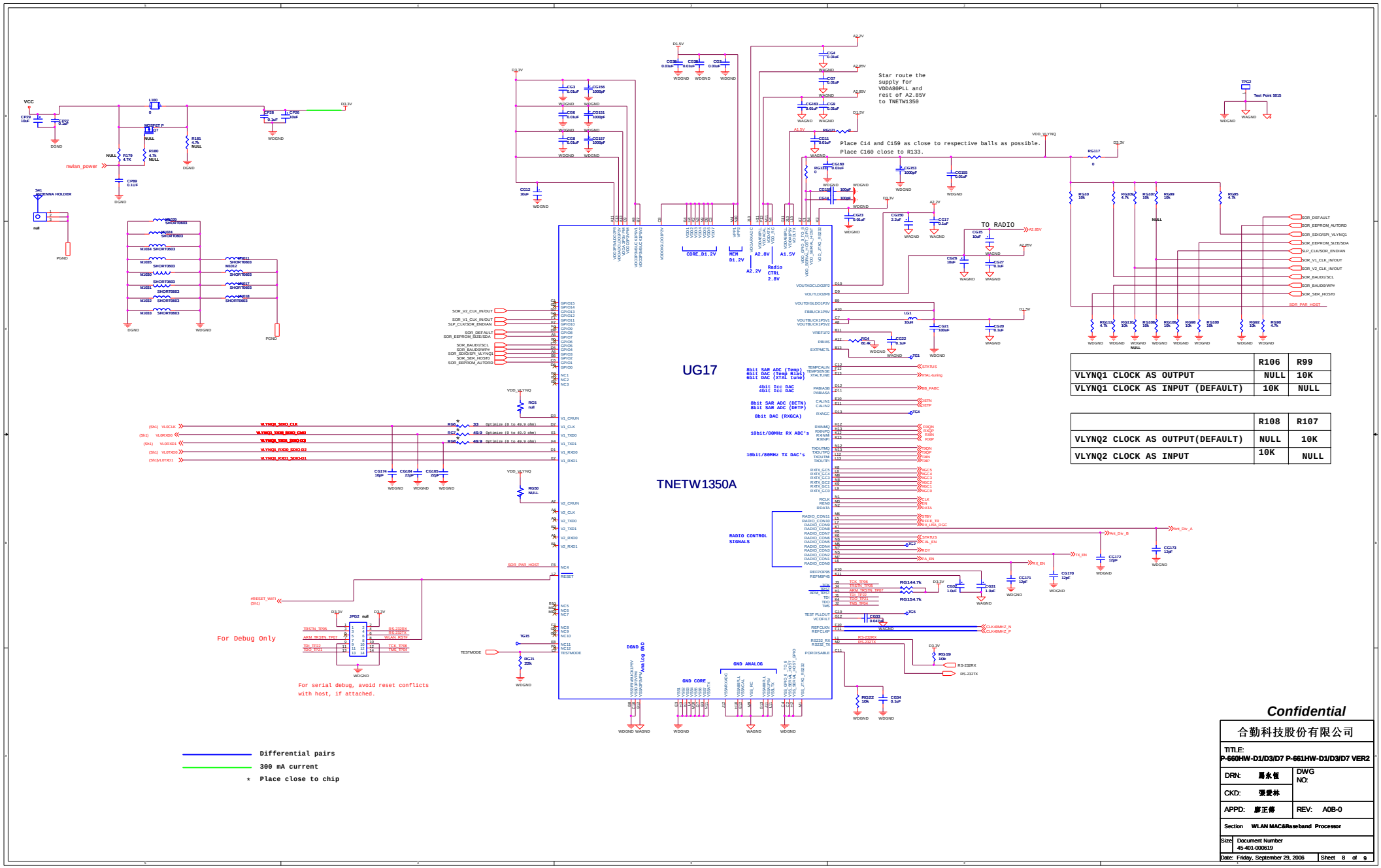

	R106	R99
VLYNQ1 CLOCK AS OUTPUT	NULL	10K
VLYNQ1 CLOCK AS INPUT (DEFAULT)	10K	NULL

	R108	R107
VLYNQ2 CLOCK AS OUTPUT(DEFAULT)	NULL	10K
VLYNQ2 CLOCK AS INPUT	10K	NULL

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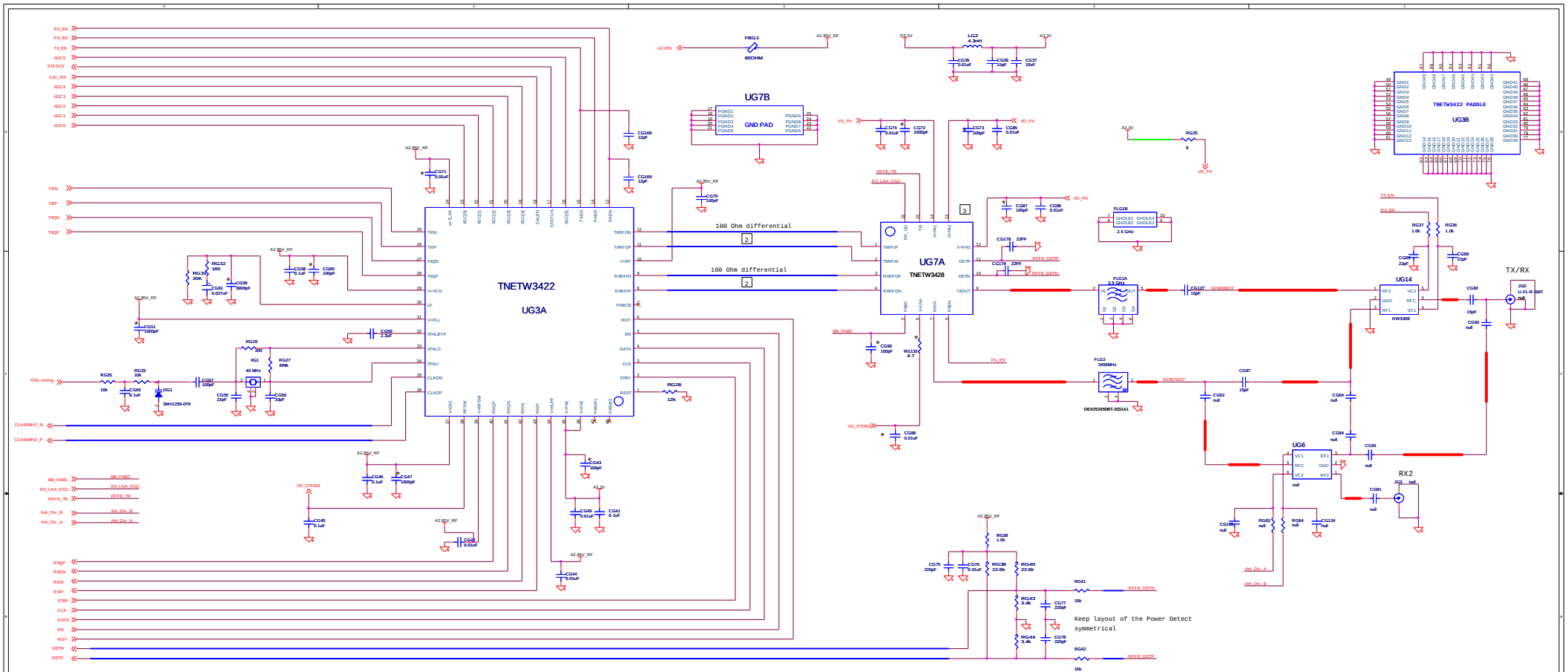
TITLE: P-660HW-D1/D3/D7 P-661HW-D1/D3/D7 VER2	
DRN: 易永恒	DWG NO:
CKD: 張愛林	
APPD: 廖正得	REV: A0B-0
Section WLAN MAC&Baseband Processor	
Size: Document Number 45-401-000619	
Date: Friday, September 29, 2006	Sheet 8 of 9



50 Ohm

Differential pairs

300 mA current

Notes:

1. *= place close to chip

2. The RF TX/RX 100 Ohm differential pairs should be symetric. BB TX I/Q differential pairs should be kept as equal as possible. Same applies for the BB RX I/Q.

3. Pins 12,13 and 14 of U7 draw high current. Insure that the trace width between above pins is wide enough to minimize the voltage drop due to trace losses.

	VD_PA=3.3V (default)	VD_PA=5V
1)C82=10UF	NULL	YES
2)C84=1UF	NULL	YES
3)C83=0.1UF	NULL	YES
4)R24=0 OHM	NULL	YES
5)R25=0 OHM	YES	NULL

	Single Antenna (default)	Two Antenna with Antenna Diversity
1)U6	null	YES
2)C81=15PF	null	YES
3)C127=15PF	YES	YES
4)U14	YES	YES
5)C69=22PF	YES	YES
6)C68=22PF	YES	YES
7)R36=1K OHM	YES	YES
8)R37=1K OHM	YES	YES
9)C92=15PF	YES	YES
10)J5	YES	YES
11)J3	null	YES
12)R63,R64=1K OHM	null	YES
13)C67=15PF	YES	null
14)C124=22PF	null	YES
15)C125=22PF	null	YES
16)C62,C64,C94=15PF	null	YES
17)C91,C93	null	null

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TITLE: P-660HW-D1/D3/D7 P-661HW-D1/D3/D7 VER2

DRN: 易永恒	DWG NO:
CKD: 張愛林	
APPD: 廖正得	REV: A0B-0
Section G-663 802.11g WLAN Module Radio	
Size: Document Number 45-401-000619A0B	
Date: Friday, September 29, 2006	Sheet 9 of 9